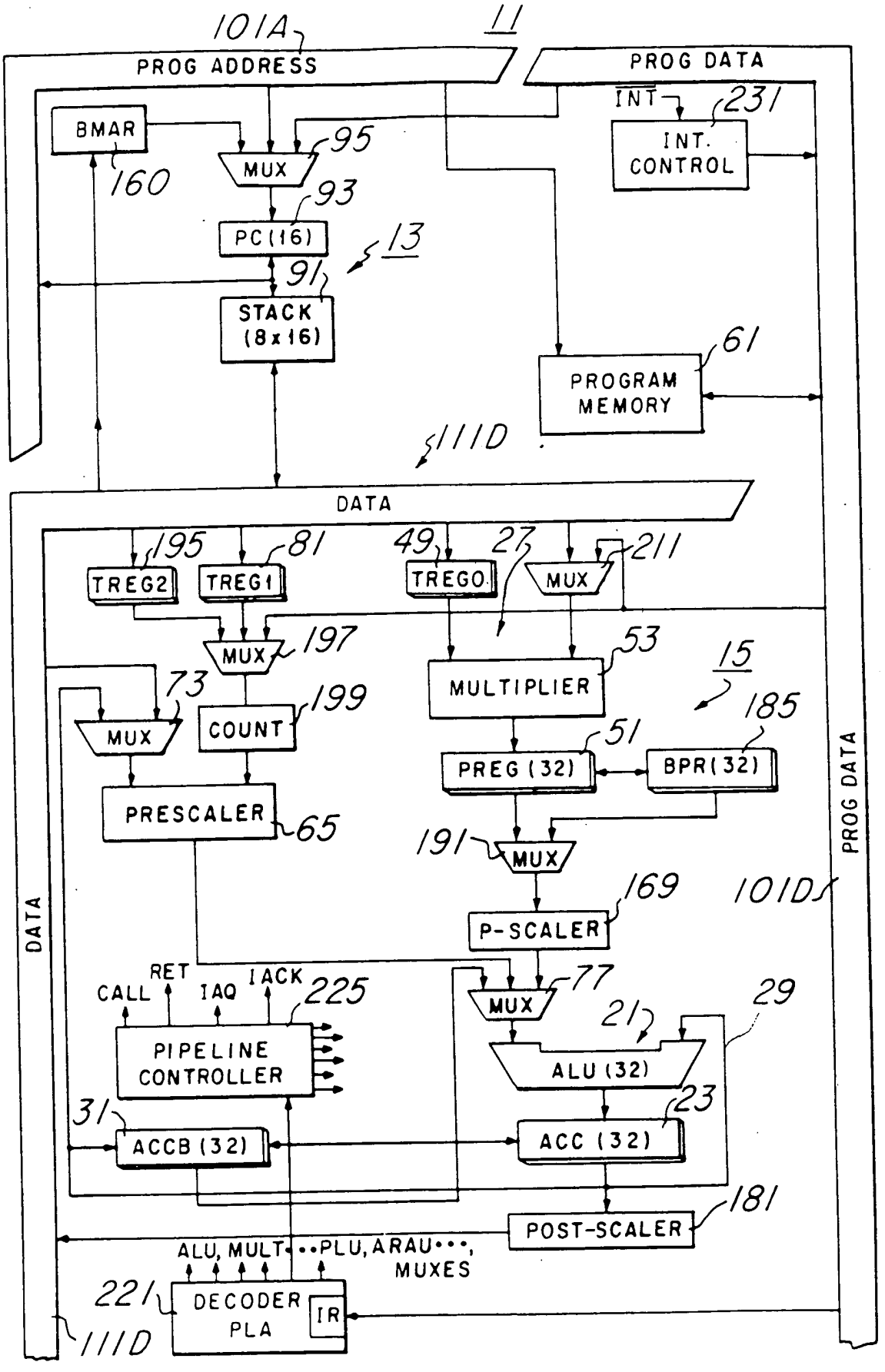

JOIN FIG.1b

Fig. 10

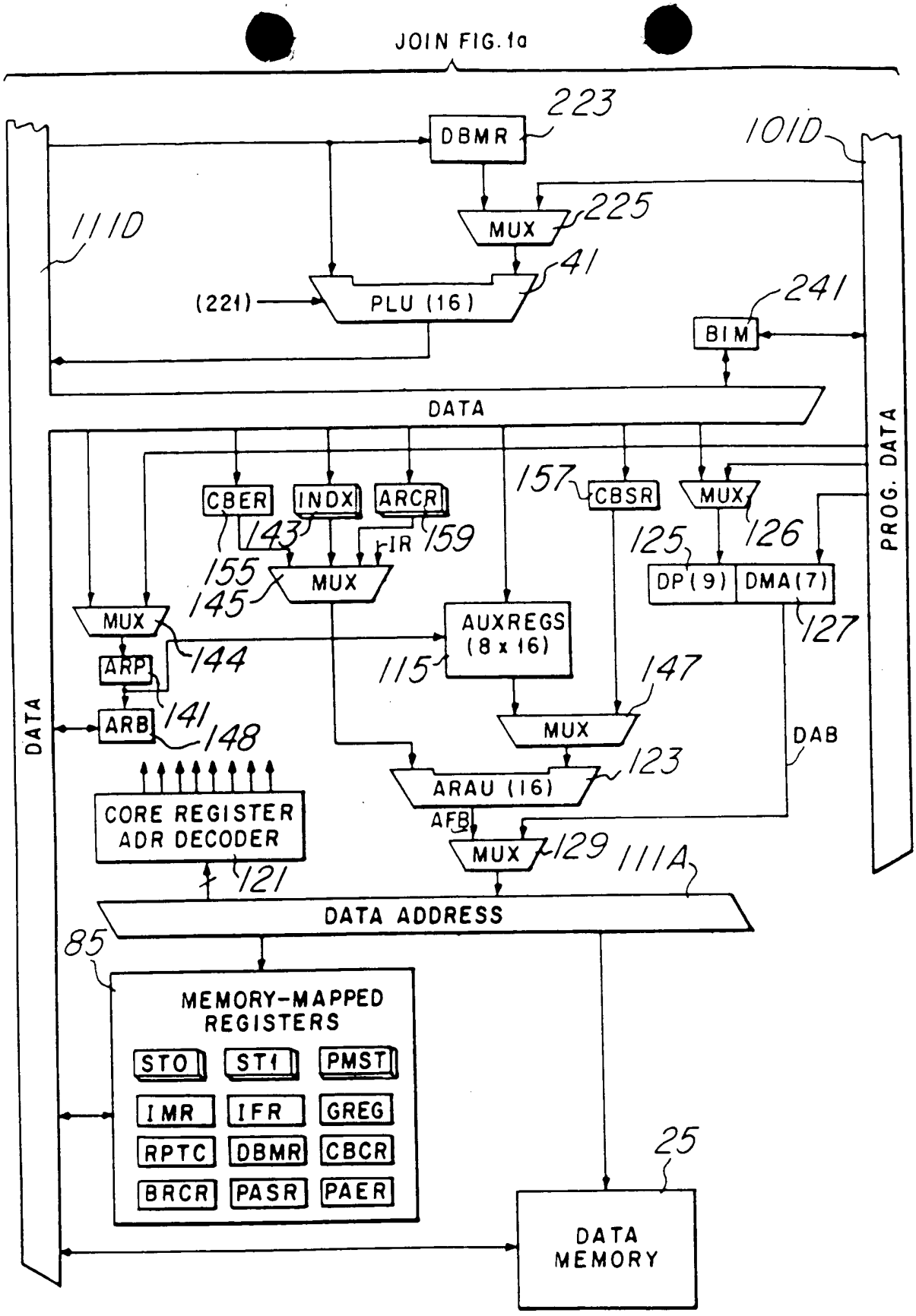
JOIN FIG. 1a
223
DBMR
101D
225
MUX
1110
41
(221)
PLU (16)
241
BIM
DATA
PROG. DATA
CBER
INDX
ARCR
157
CBSR
MUX
143
IR
159
125
126
155
MUX
DP (9)
DMA (7)
145
MUX
AUXREGS (8 x 16)
127
144
115
147
ARP
141
MUX
DATA
ARB
148
DAB
123
ARAU (16)
CORE REGISTER ADR DECODER
AFB
MUX
129
111A
121
DATA ADDRESS
85
MEMORY-MAPPED REGISTERS
STO
ST1
PMST
IMR
IFR
GREG
RPTC
DBMR
CBCR
BRCR
PASR
PAER
25
DATA MEMORY

Fig. 1b

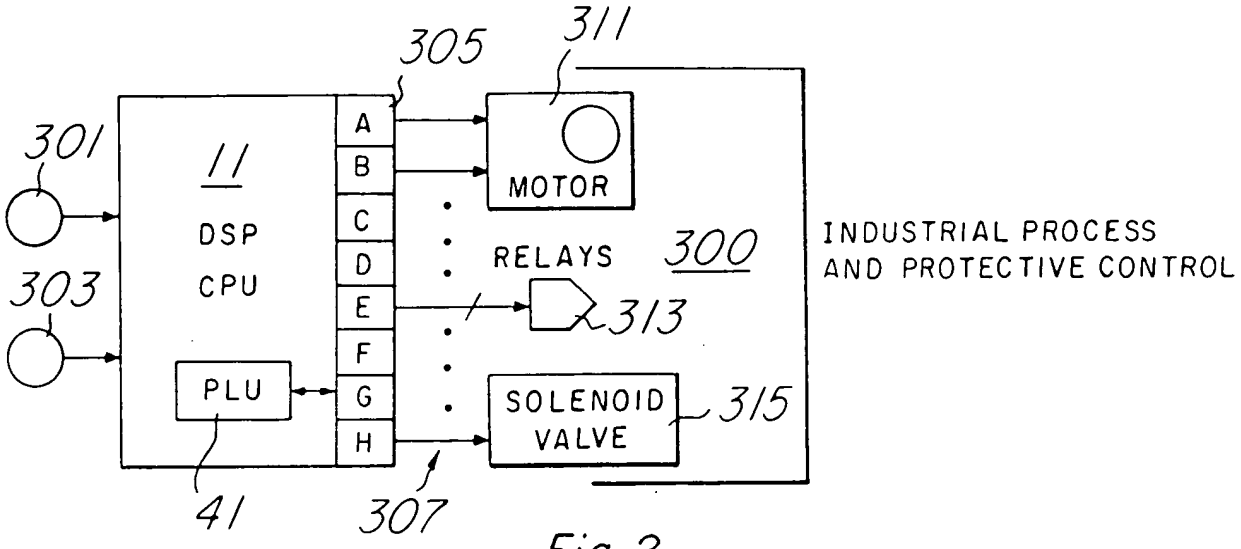

Fig. 2

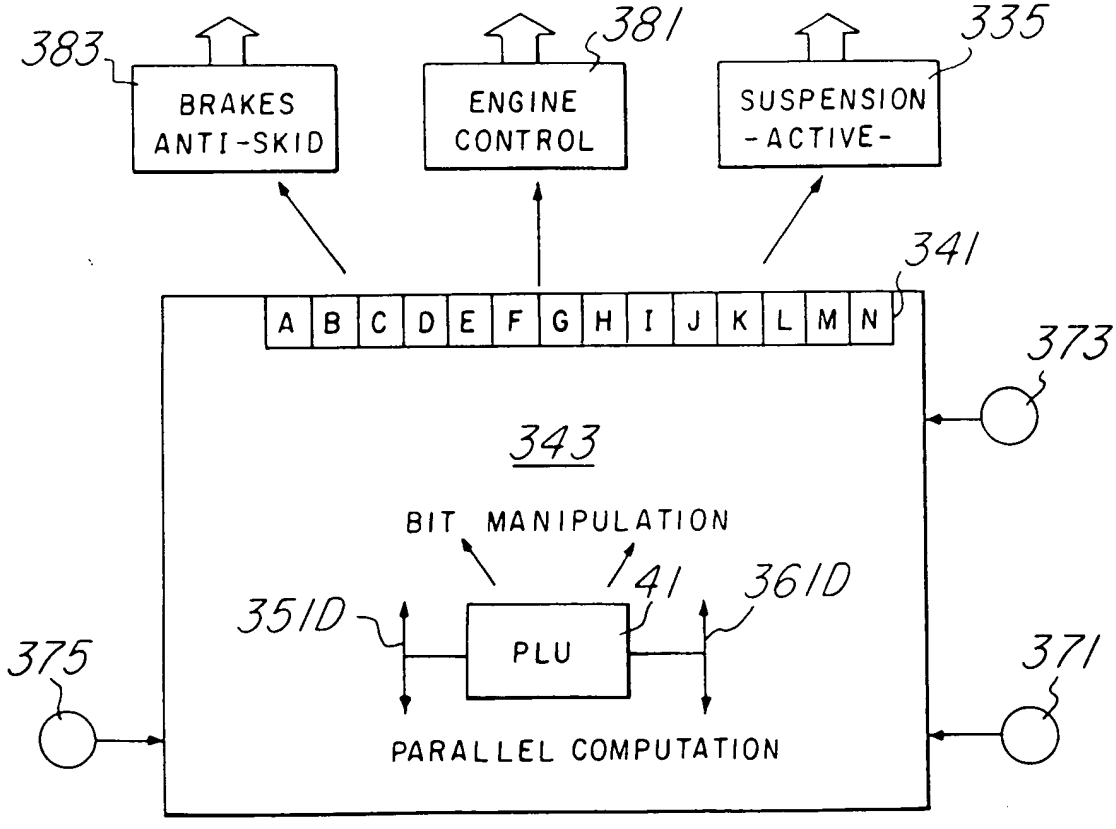

Fig. 3

D0604400-0604628

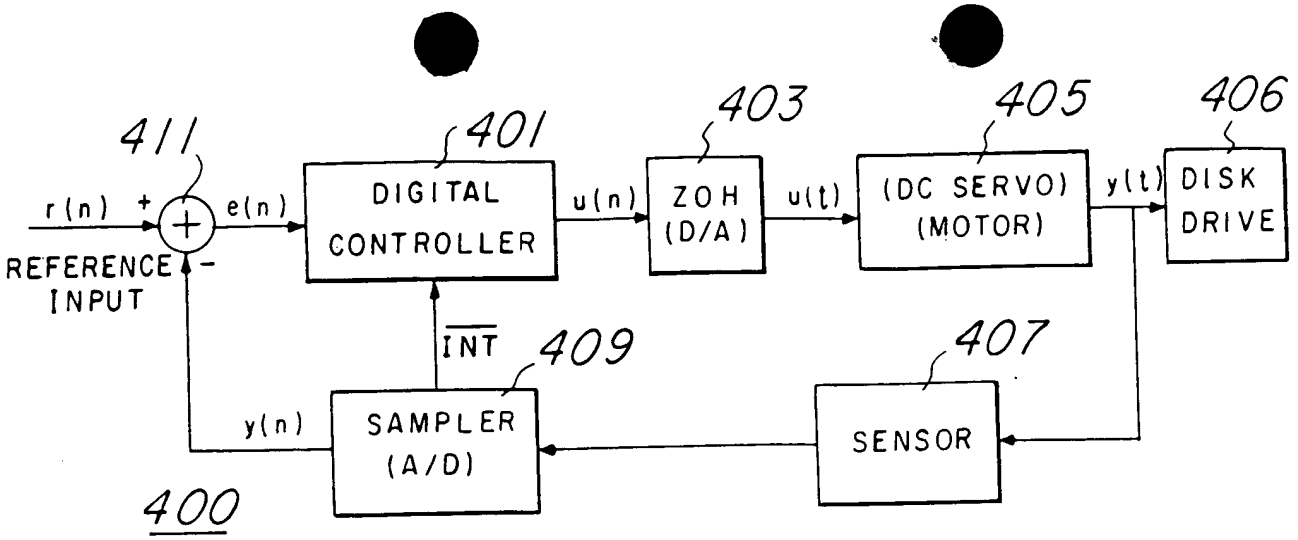

Fig. 4

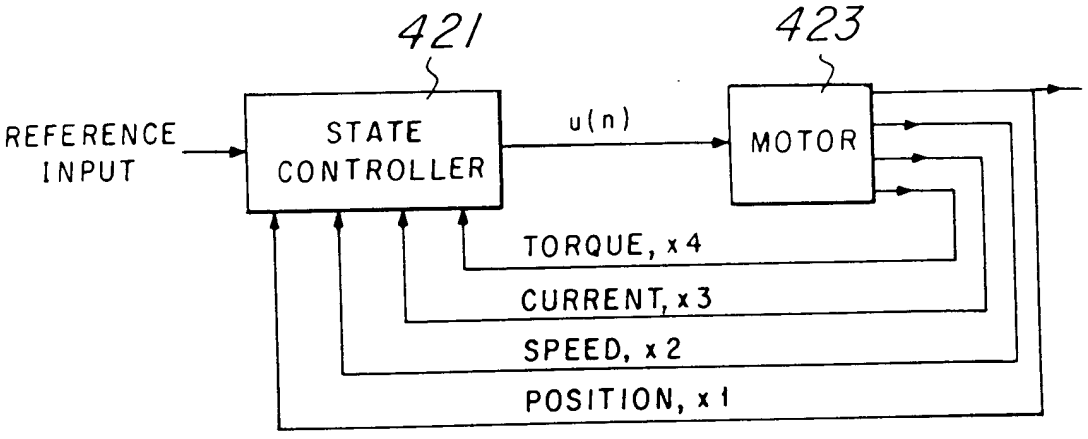

Fig. 5

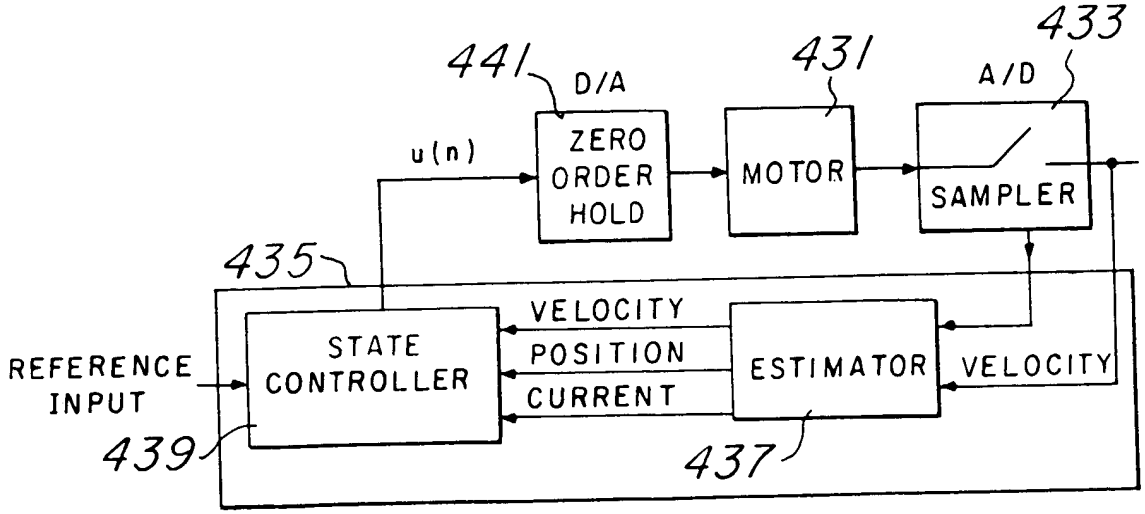

Fig. 6

00T60"82229960

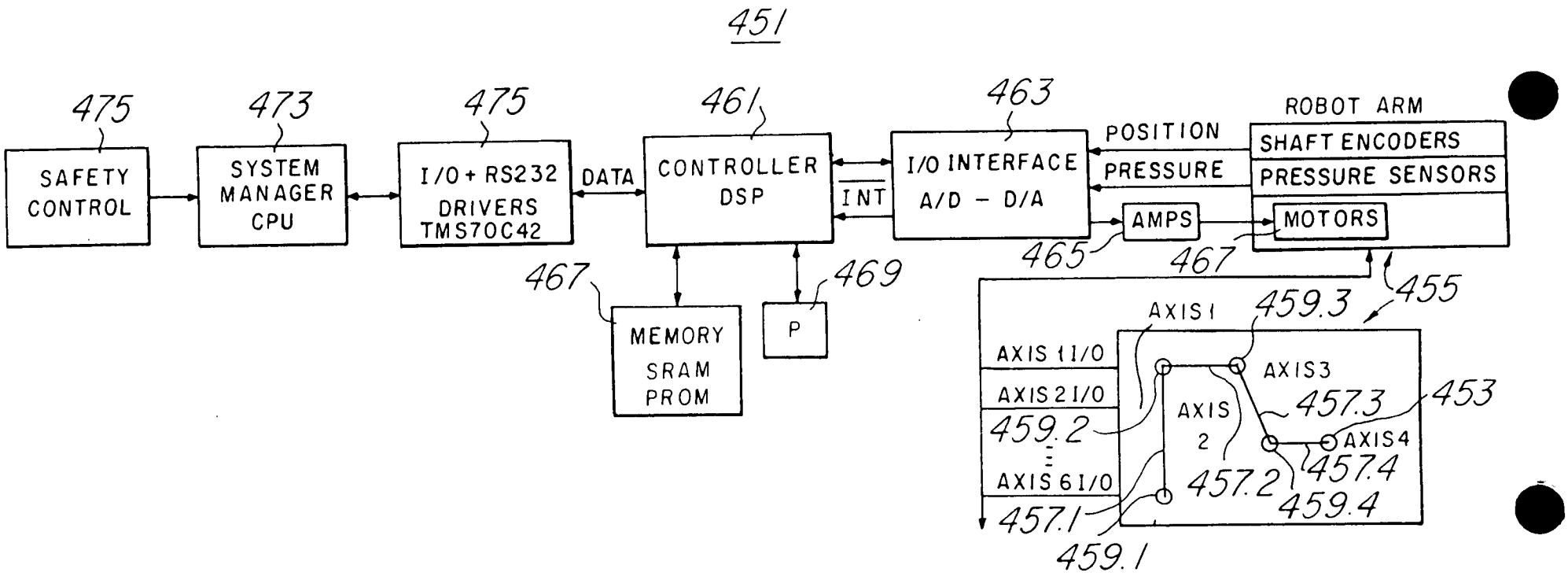

Fig. 7

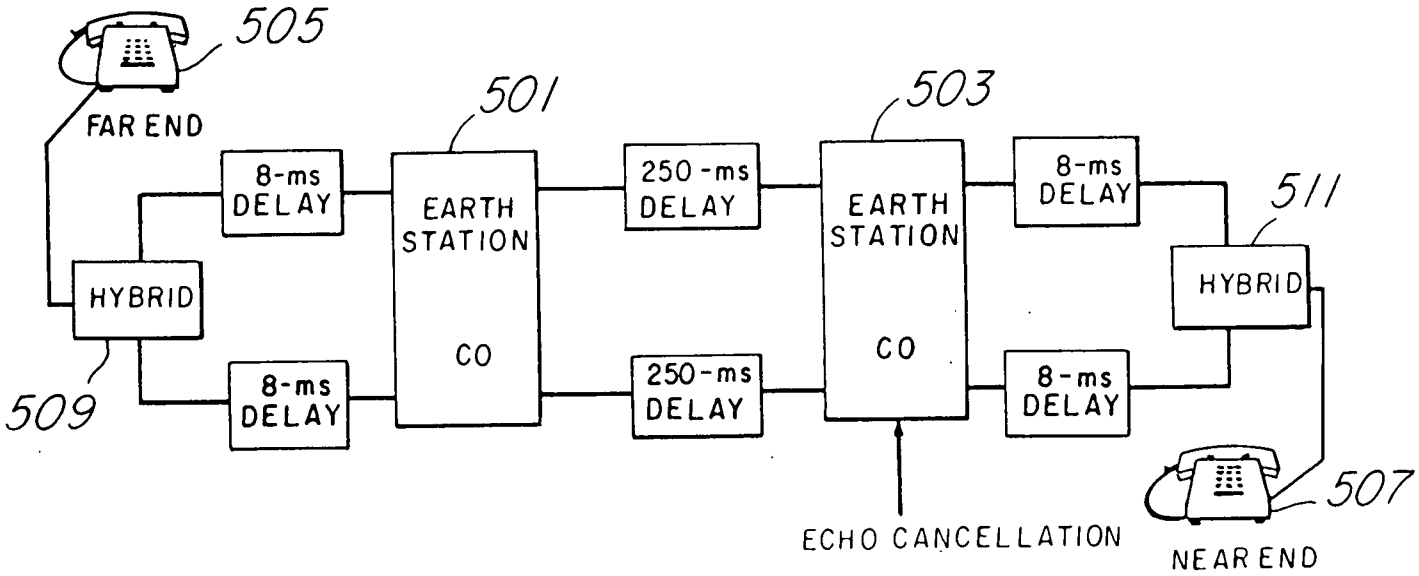
505
FAR END
501
503
8-ms DELAY
EARTH STATION
CO
250-ms DELAY
EARTH STATION
CO
8-ms DELAY
511
HYBRID
HYBRID
509
8-ms DELAY
250-ms DELAY
8-ms DELAY
ECHO CANCELLATION
507
NEAR END

Fig. 8

00T60"8229960

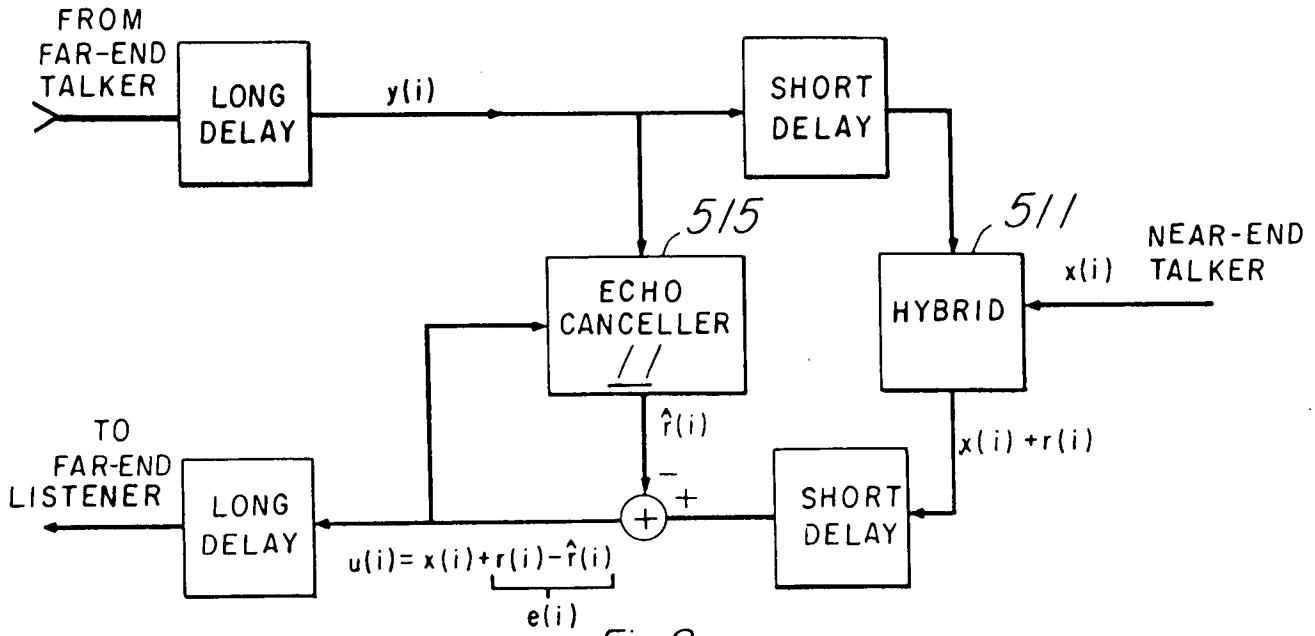

Fig.9

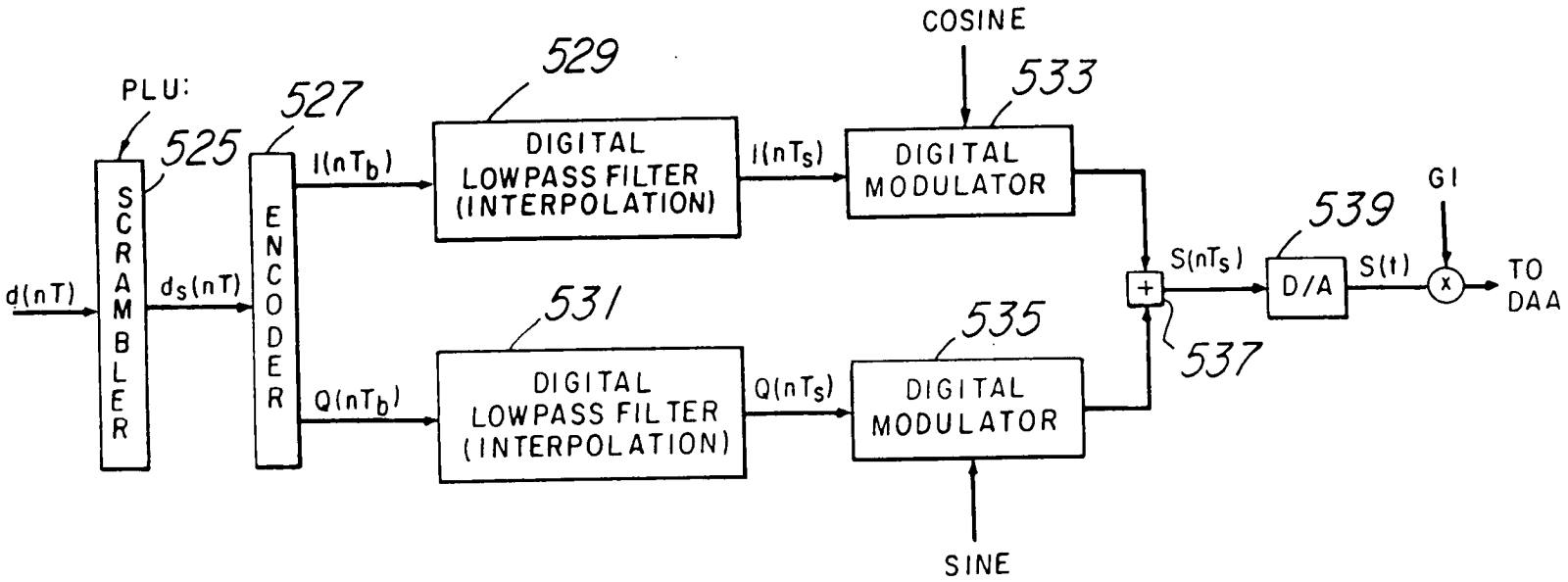
PLU:
525
SCRAMBLER
d(nT)
ds(nT)
527
ENCODER
I(nTb)
Q(nTb)
529
DIGITAL LOWPASS FILTER (INTERPOLATION)
531
DIGITAL LOWPASS FILTER (INTERPOLATION)
I(nTs)
Q(nTs)
COSINE
533
DIGITAL MODULATOR
535
DIGITAL MODULATOR
SINE
+
537
S(nTs)
539
D/A
S(t)
GI
X
TO DAA

Fig. 10

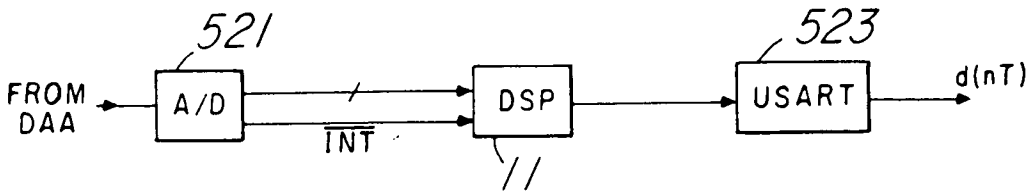
521
523
FROM DAA
A/D
INT
DSP
USART
d(nT)
//

Fig. 11

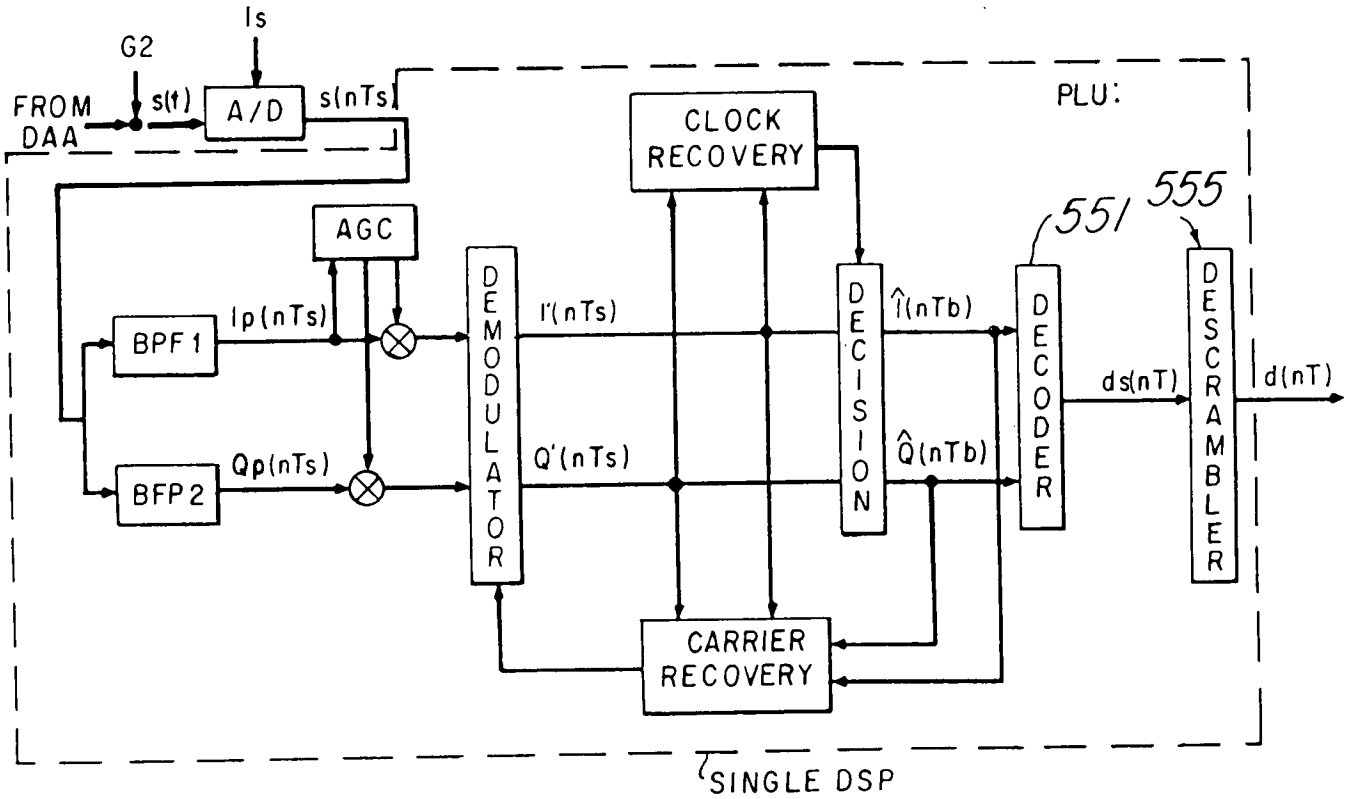
Is
G2
FROM DAA
s(t)
A/D
s(nTs)
PLU:
CLOCK RECOVERY
AGC
551
555
BPF 1
Ip(nTs)
DEMODULATOR
I'(nTs)
DECISION
Î(nTb)
DECODER
ds(nT)
DESCRAMBLER
d(nT)
BFP2
Qp(nTs)
Q'(nTs)
Q̂(nTb)
CARRIER RECOVERY
SINGLE DSP

Fig. 12

00760 8229960

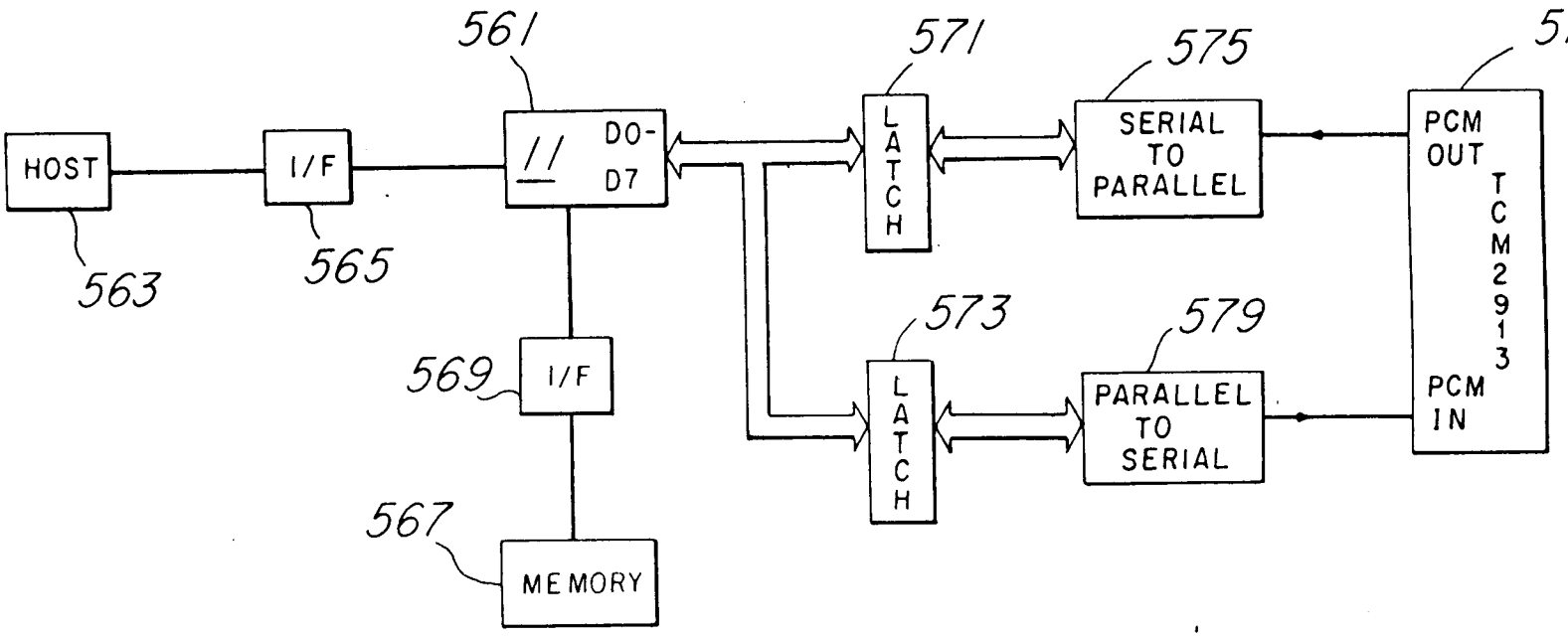

Fig. 13

00T60"822886O

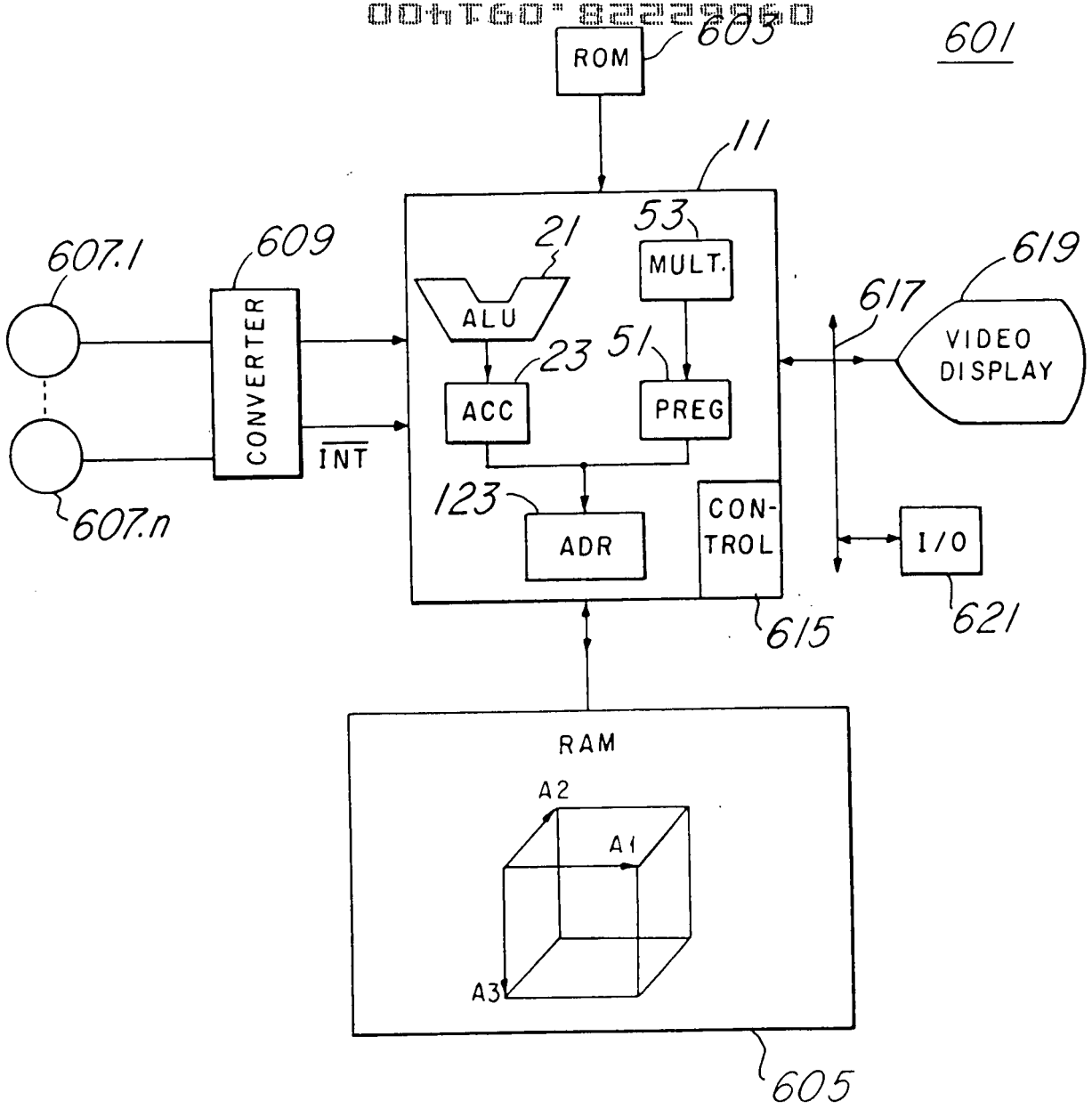

Fig. 14

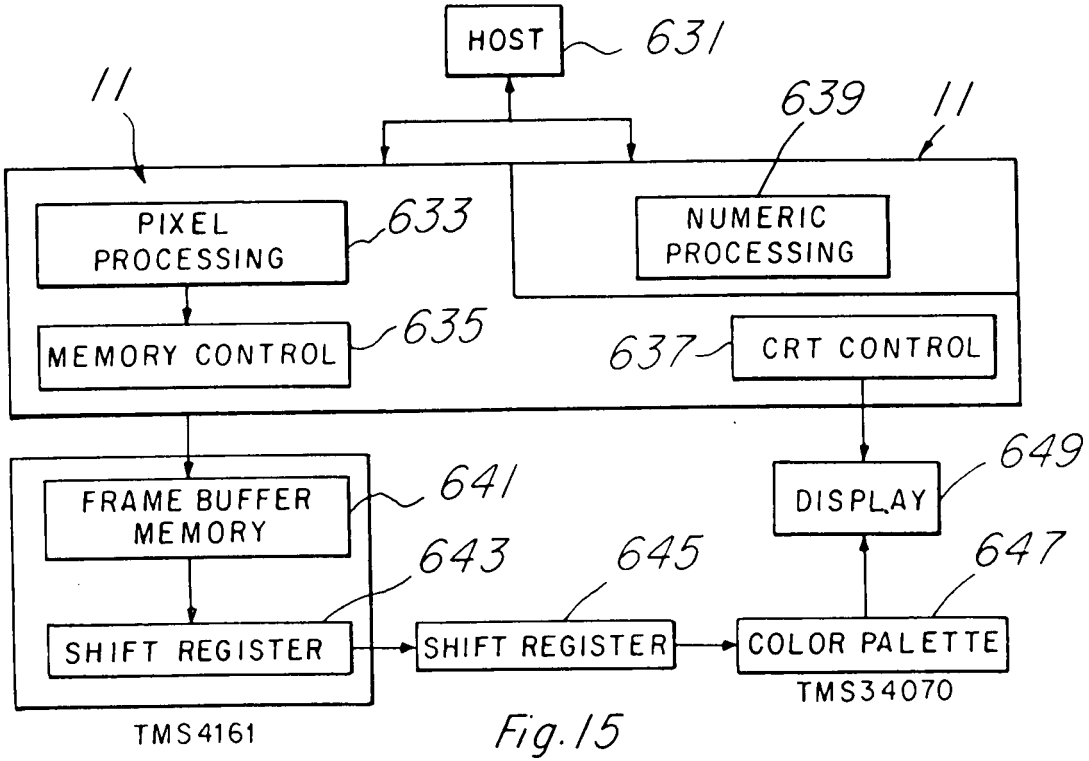
HOST
631
11
639
11
PIXEL PROCESSING
633
NUMERIC PROCESSING
MEMORY CONTROL
635
637
CRT CONTROL
FRAME BUFFER MEMORY
641
649
DISPLAY
643
645
647
SHIFT REGISTER
SHIFT REGISTER
COLOR PALETTE
TMS34070
TMS4161

Fig. 15

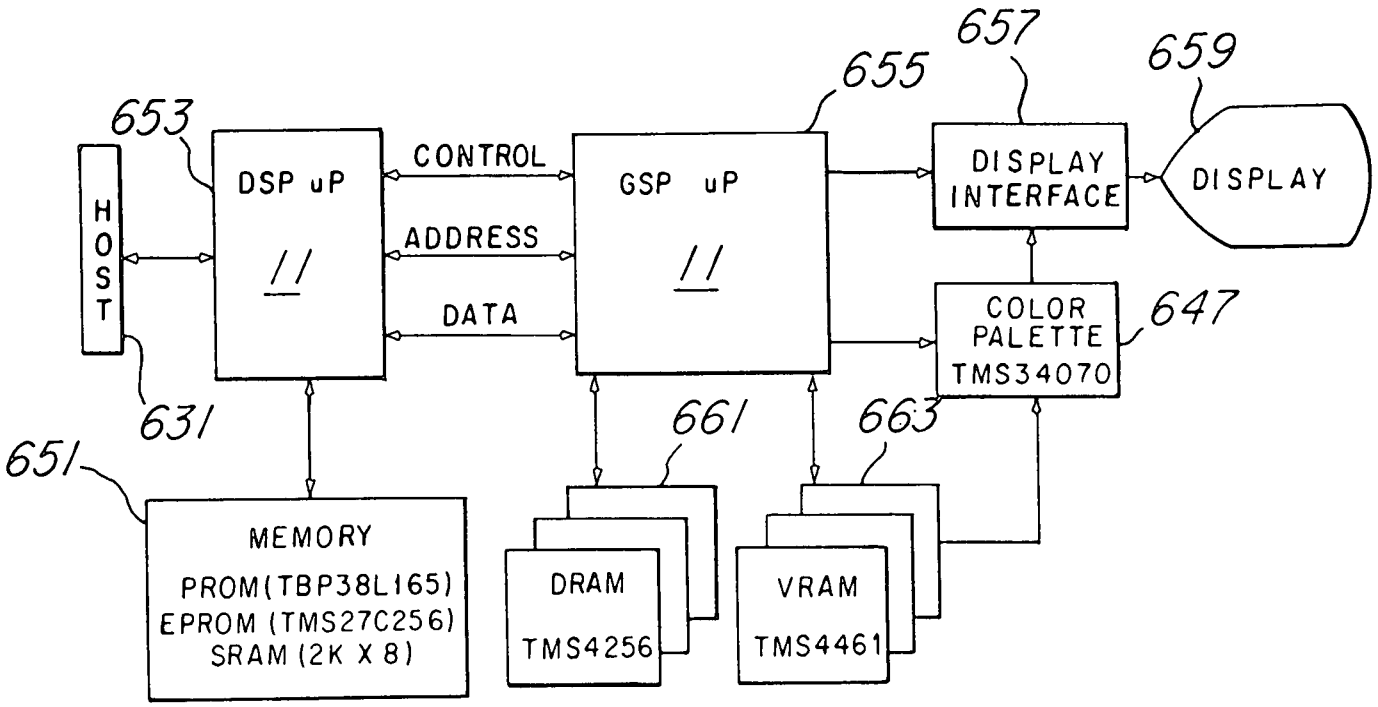
653
655
657
659
HOST
DSP uP
//
CONTROL
ADDRESS
DATA
GSP uP
//
DISPLAY INTERFACE
DISPLAY
COLOR PALETTE TMS34070
647
631
651
661
663
MEMORY
PROM(TBP38L165)
EPROM (TMS27C256)
SRAM (2K X 8)
DRAM
TMS4256
VRAM
TMS4461

Fig. 16

DOHT60 "8229960

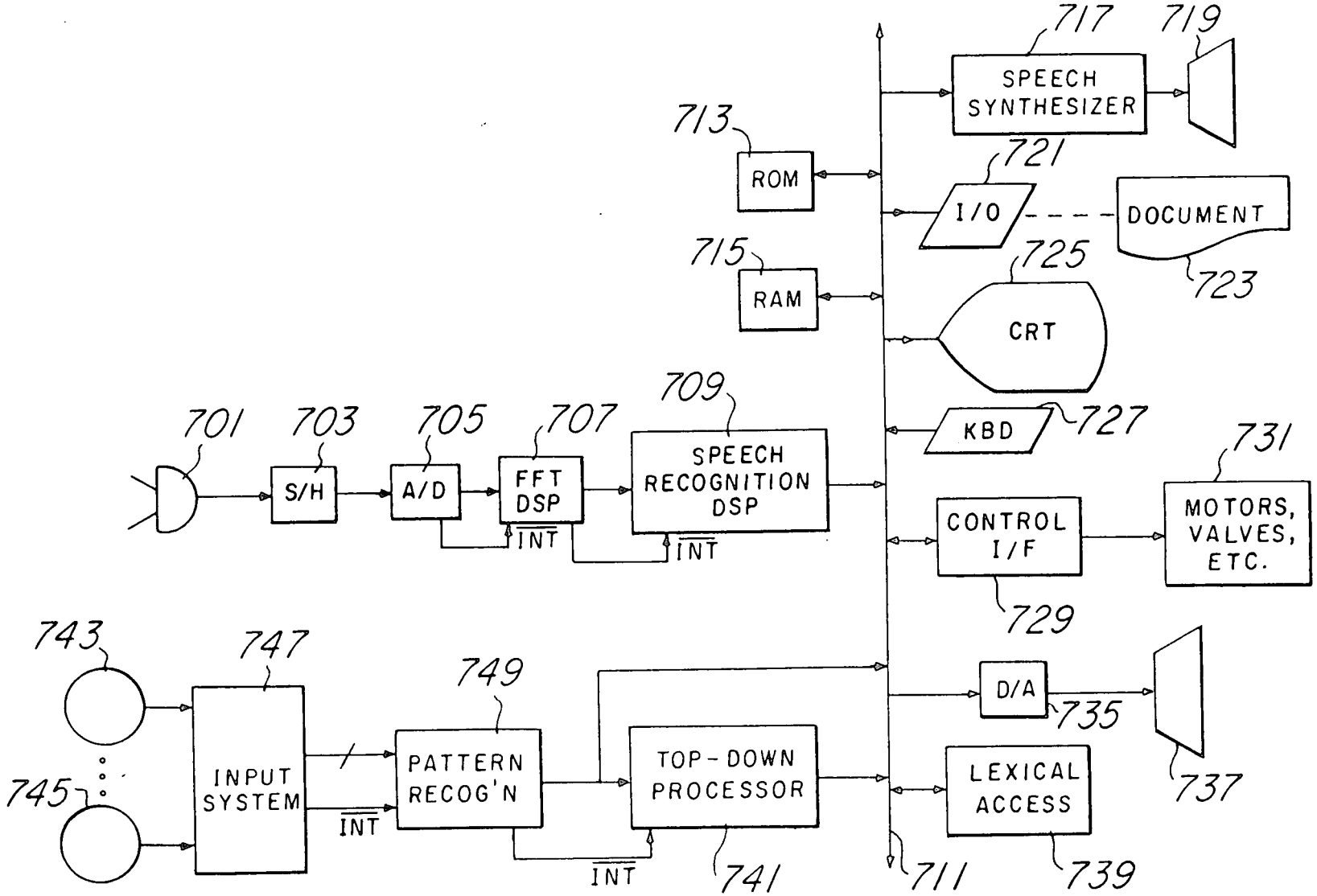

Fig.17

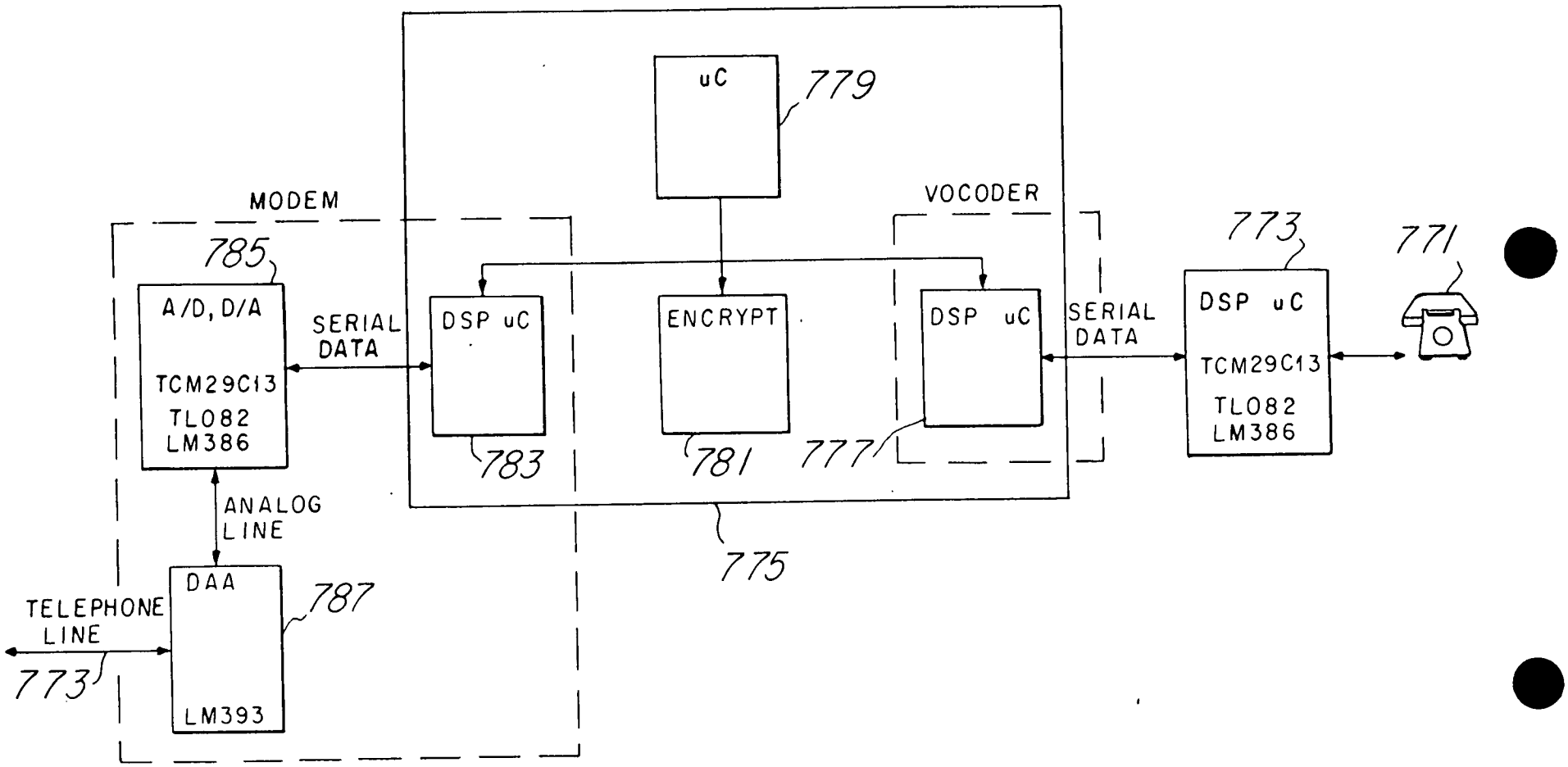
uC
779
MODEM
VOCODER
785
773
771
A/D, D/A
TCM29C13
TL082
LM386
SERIAL DATA
DSP uC
ENCRYPT
DSP uC
SERIAL DATA
DSP uC
TCM29C13
TL082
LM386
783
781
777
ANALOG LINE
775
DAA
787
TELEPHONE LINE
773
LM393

Fig. 18

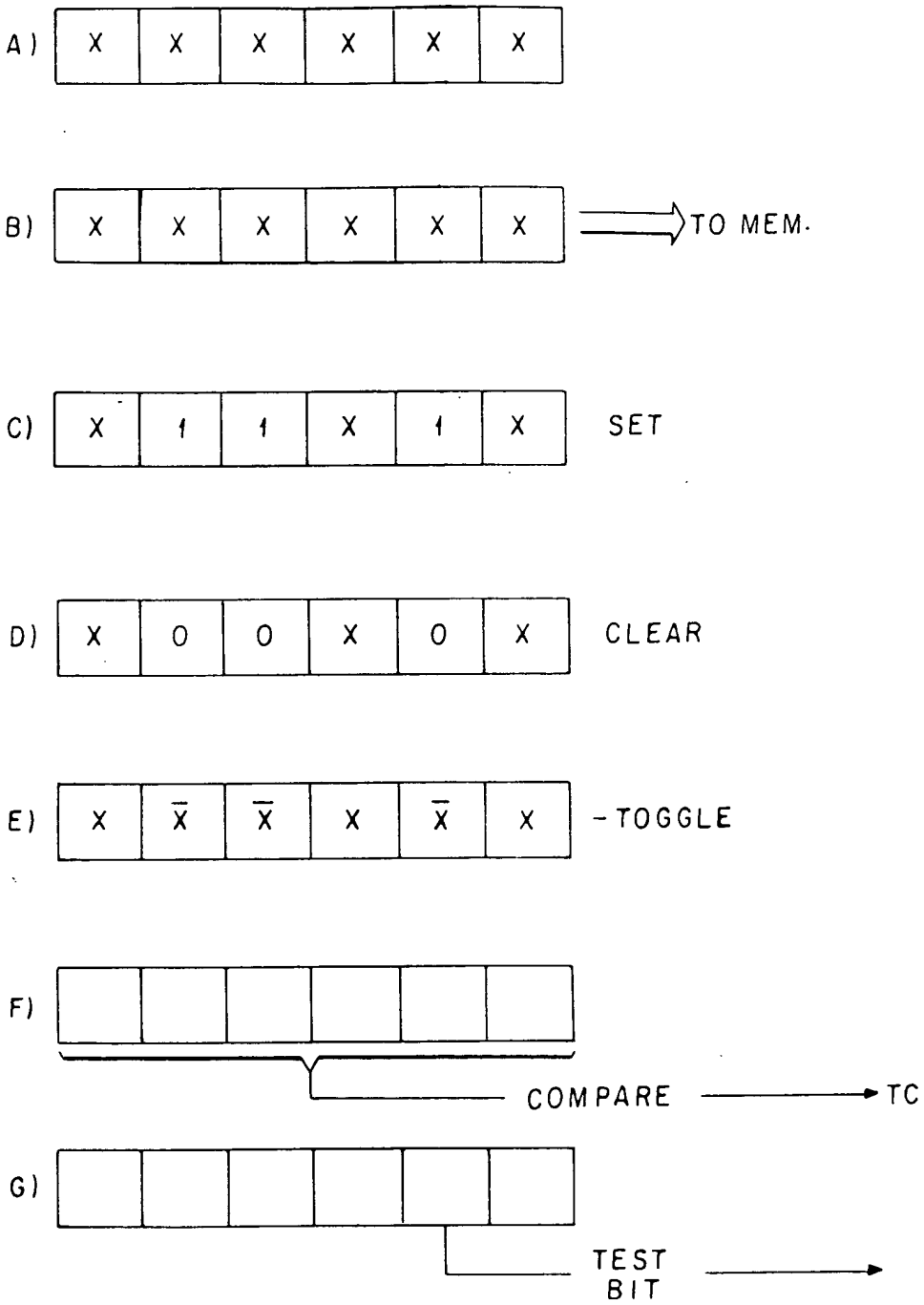
A)
X X X X X X
B)
X X X X X X
TO MEM.
C)
X 1 1 X 1 X
SET
D)
X 0 0 X 0 X
CLEAR
E)
X $\overline{X}$ $\overline{X}$ X $\overline{X}$ X
-TOGGLE
F)
COMPARE
TC
G)
TEST
BIT

Fig. 19

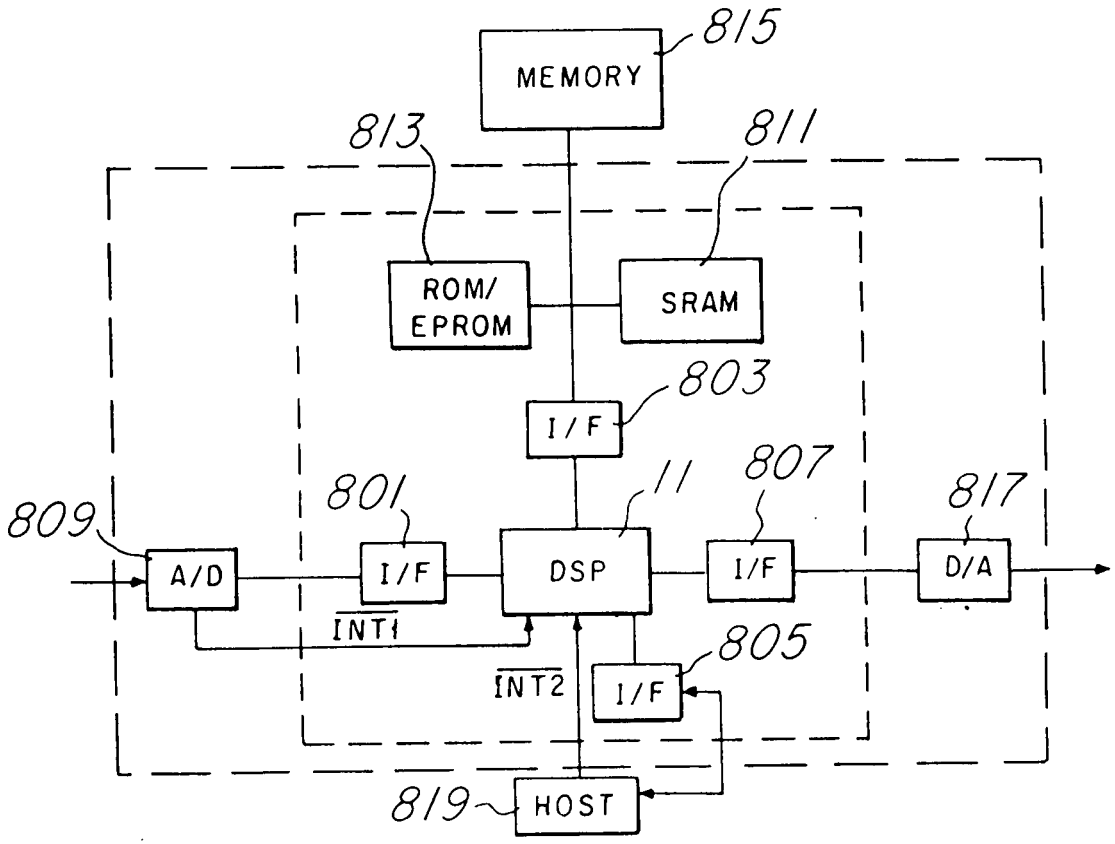
MEMORY
815
813
811
ROM/
EPROM
SRAM
803
I/F
807
11
801
809
817
A/D
I/F
DSP
I/F
D/A
INT1
805
INT2
I/F
819
HOST

Fig. 20

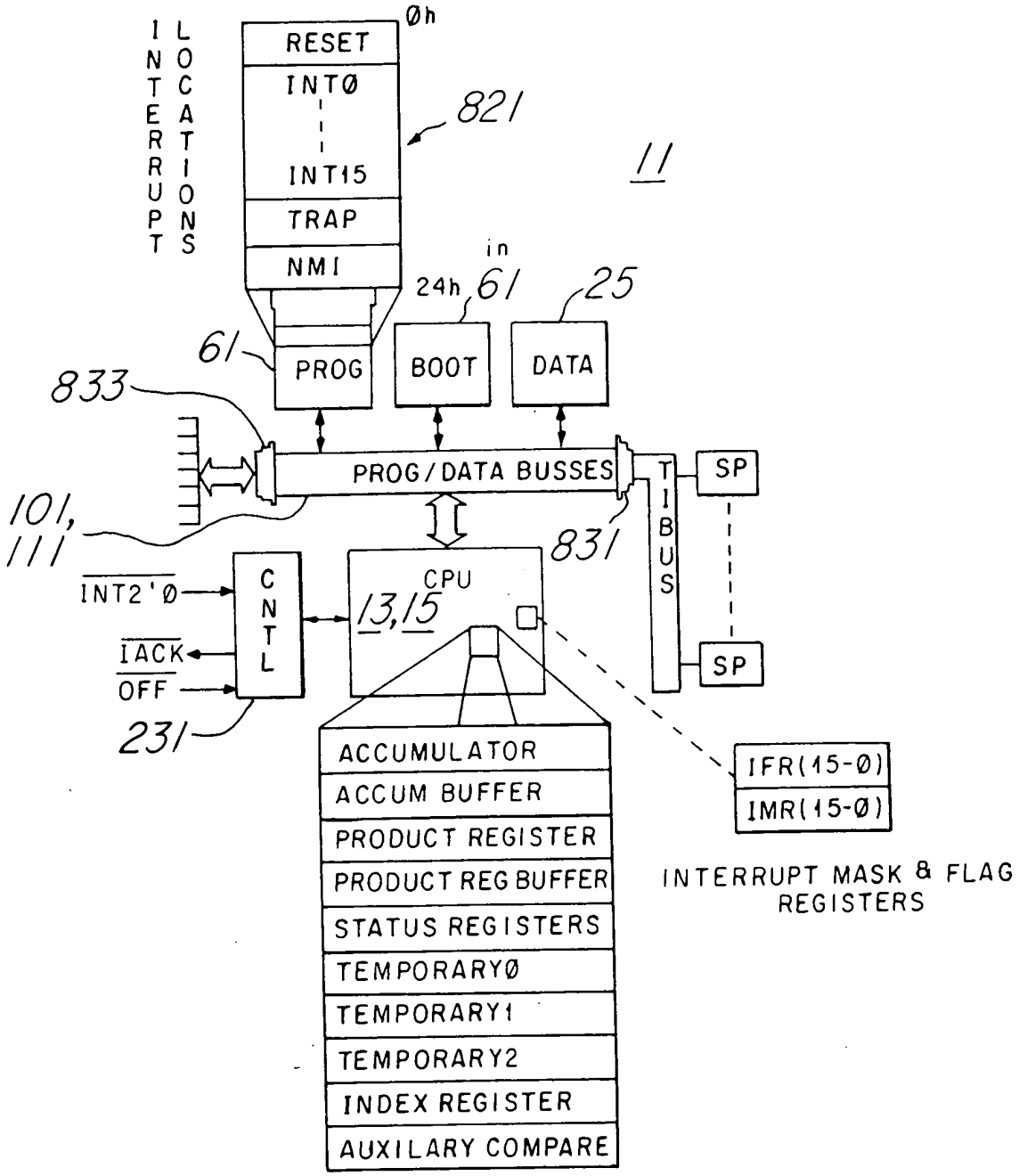
INTERRUPT LOCATIONS
RESET
INT0
INT15
TRAP
NMI
0h
821
11
in
24h
61
25
61
PROG
BOOT
DATA
833
PROG/DATA BUSSES
TIBUS
SP
SP
101,
111
831
INT2'0
IACK
OFF
CNTL
CPU
13,15
231
ACCUMULATOR
ACCUM BUFFER
PRODUCT REGISTER
PRODUCT REG BUFFER
STATUS REGISTERS
TEMPORARY0
TEMPORARY1
TEMPORARY2
INDEX REGISTER
AUXILARY COMPARE
IFR(15-0)
IMR(15-0)
INTERRUPT MASK & FLAG REGISTERS

Fig. 21

0054600.0054700

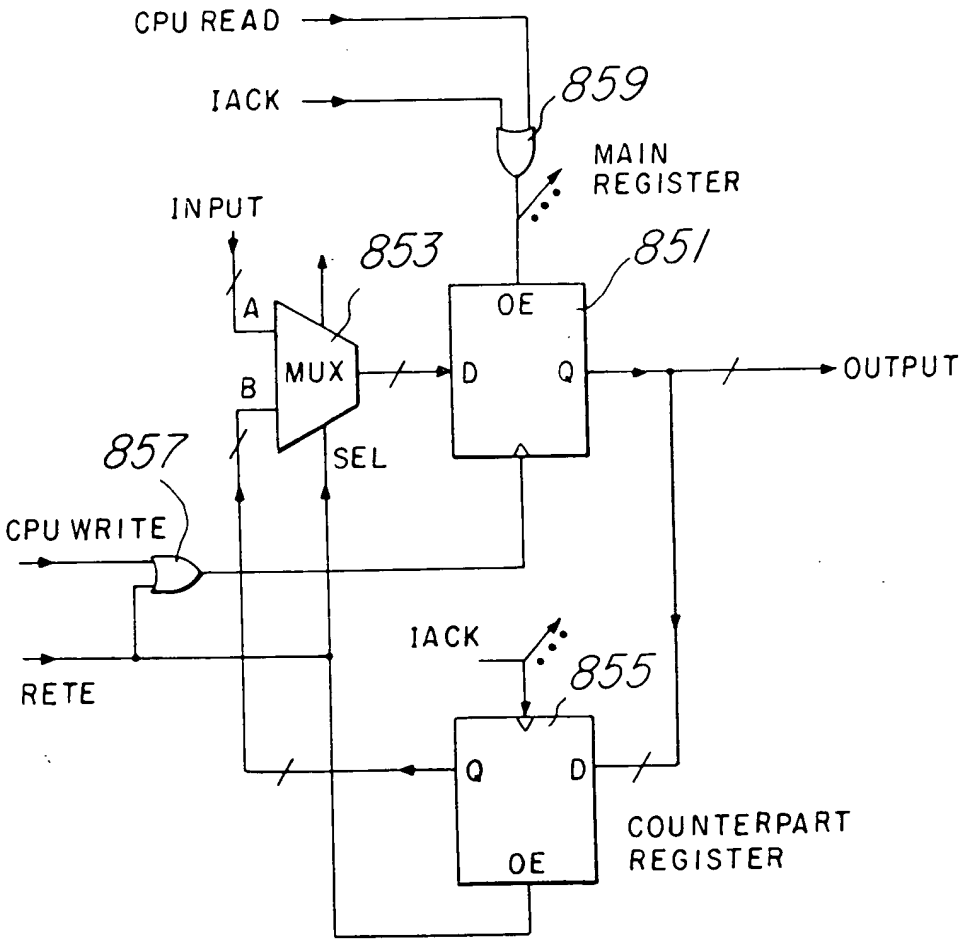

Fig. 22

00h160" 8222960

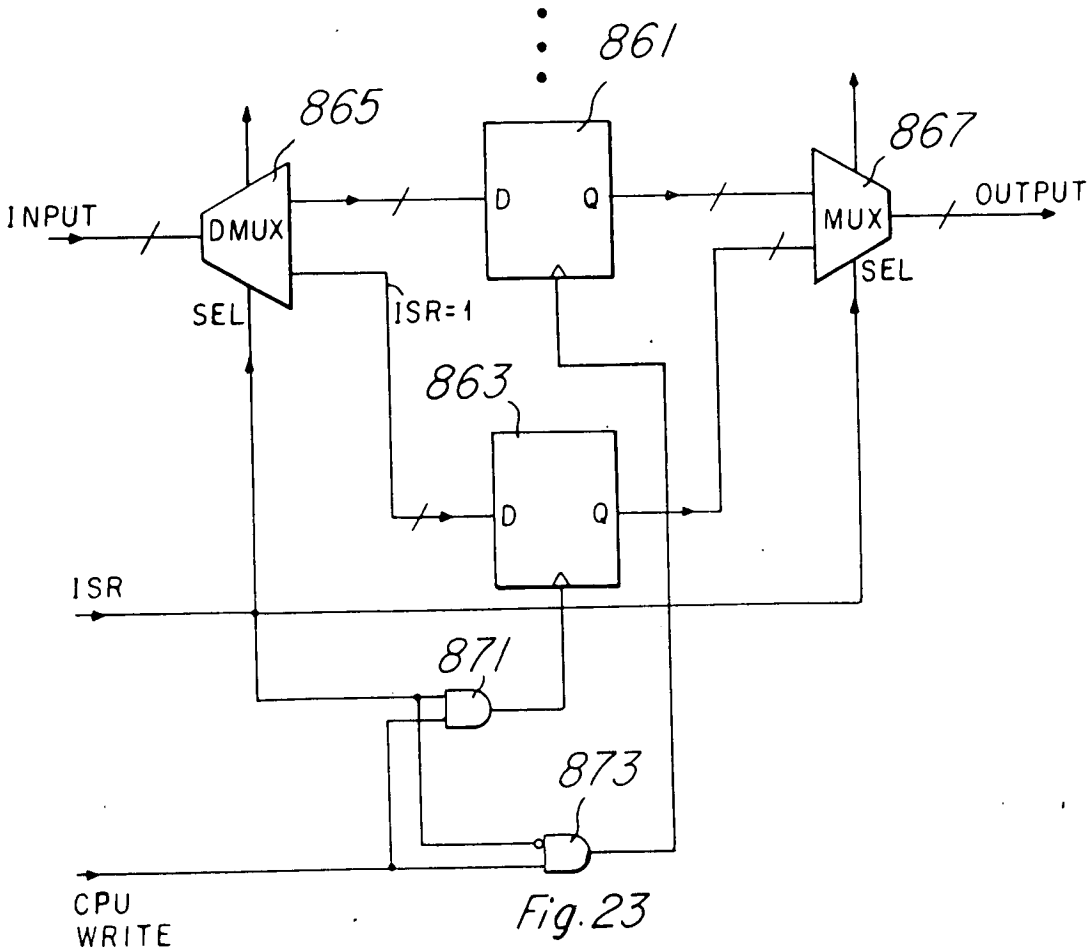

Fig. 23

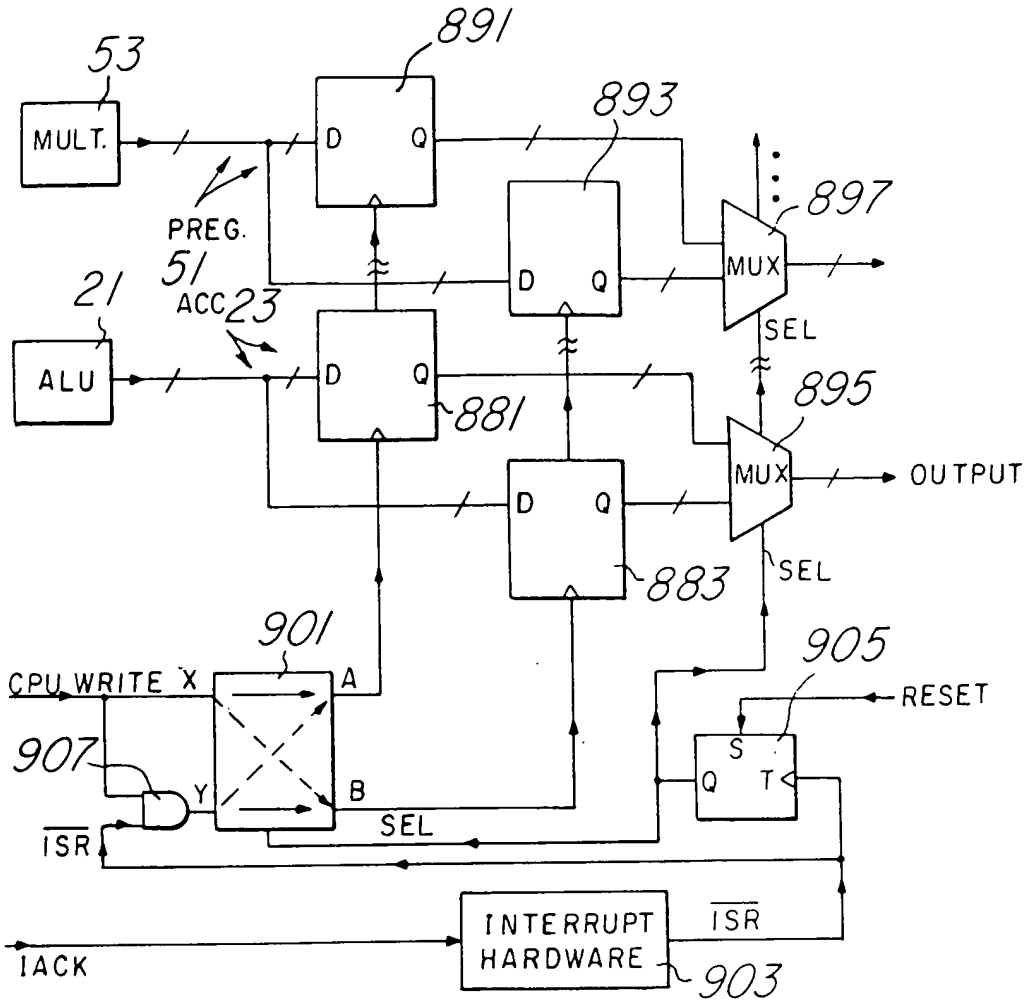
53
MULT.
891
893
897
PREG.
51
ACC
23
21
ALU
D
Q
MUX
SEL
881
895
OUTPUT
883
901
905
CPU WRITE X
A
RESET
907
Y
B
S
Q
T
SEL
ISR
INTERRUPT HARDWARE
ISR
IACK
903

Fig. 24

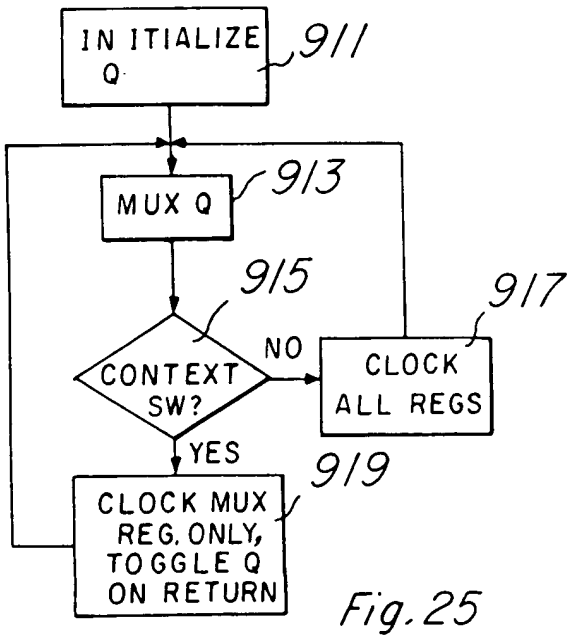
IN ITIALIZE Q
911
MUX Q
913
915
917
CONTEXT SW?
NO
CLOCK ALL REGS
YES
919
CLOCK MUX REG. ONLY, TOGGLE Q ON RETURN

Fig. 25

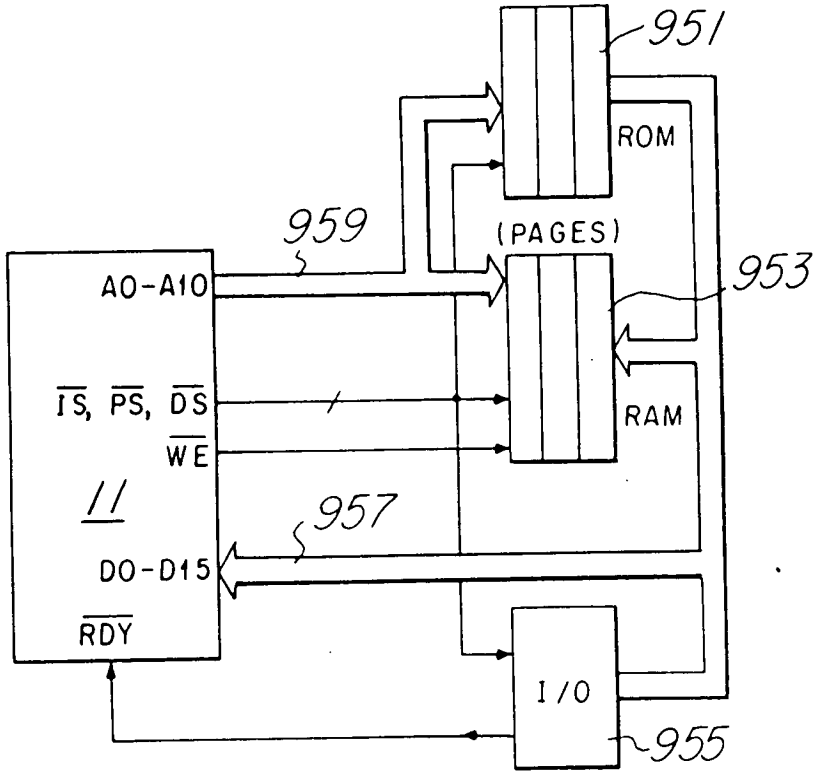

Fig. 26

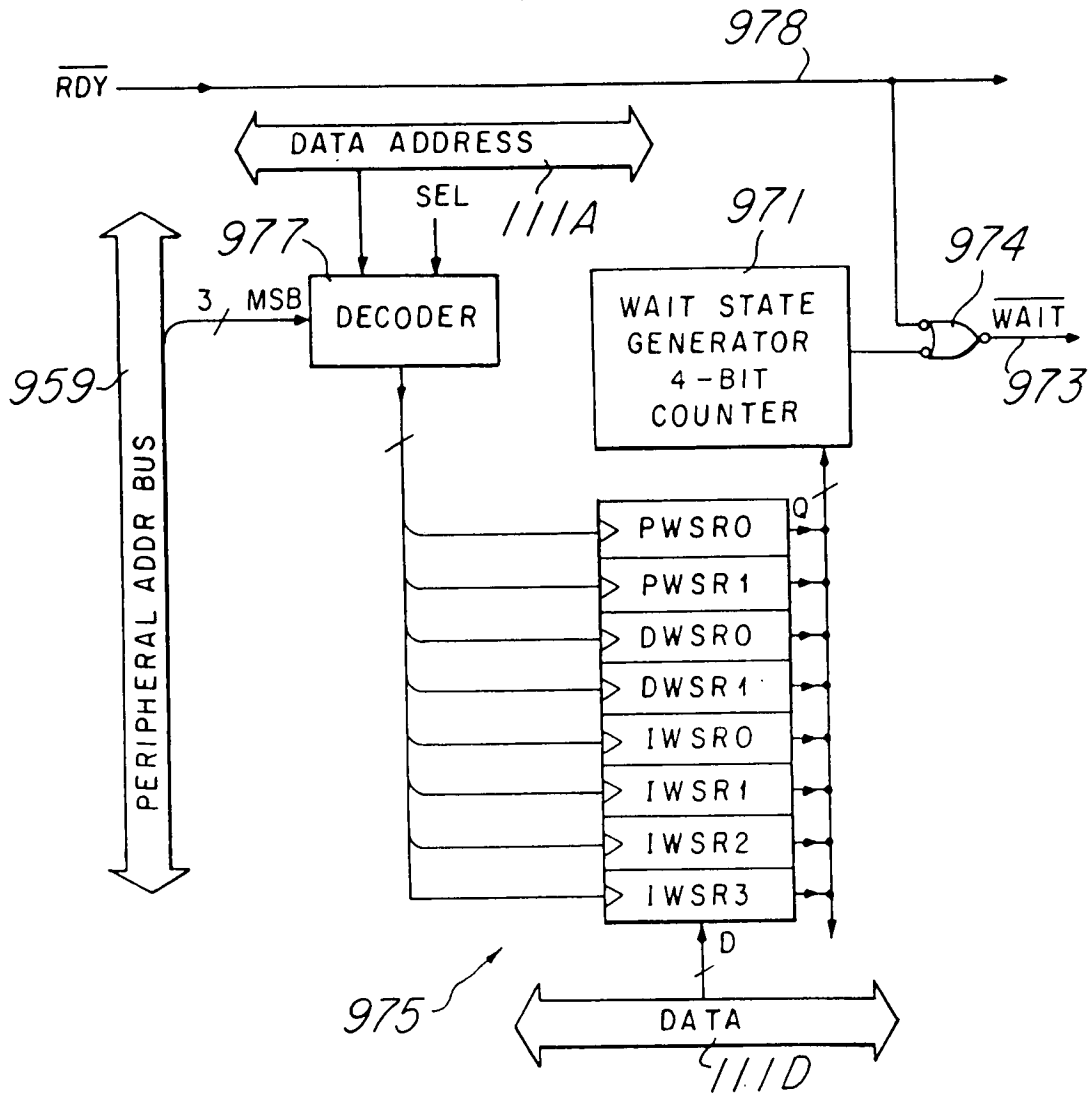
978
RDY
DATA ADDRESS
SEL
111A
971
977
974
3 MSB
DECODER
WAIT STATE GENERATOR 4-BIT COUNTER
WAIT
959
973
PERIPHERAL ADDR BUS
Q
PWSR0
PWSR1
DWSR0
DWSR1
IWSR0
IWSR1
IWSR2
IWSR3
D
975
DATA
111D

Fig. 27

0047400

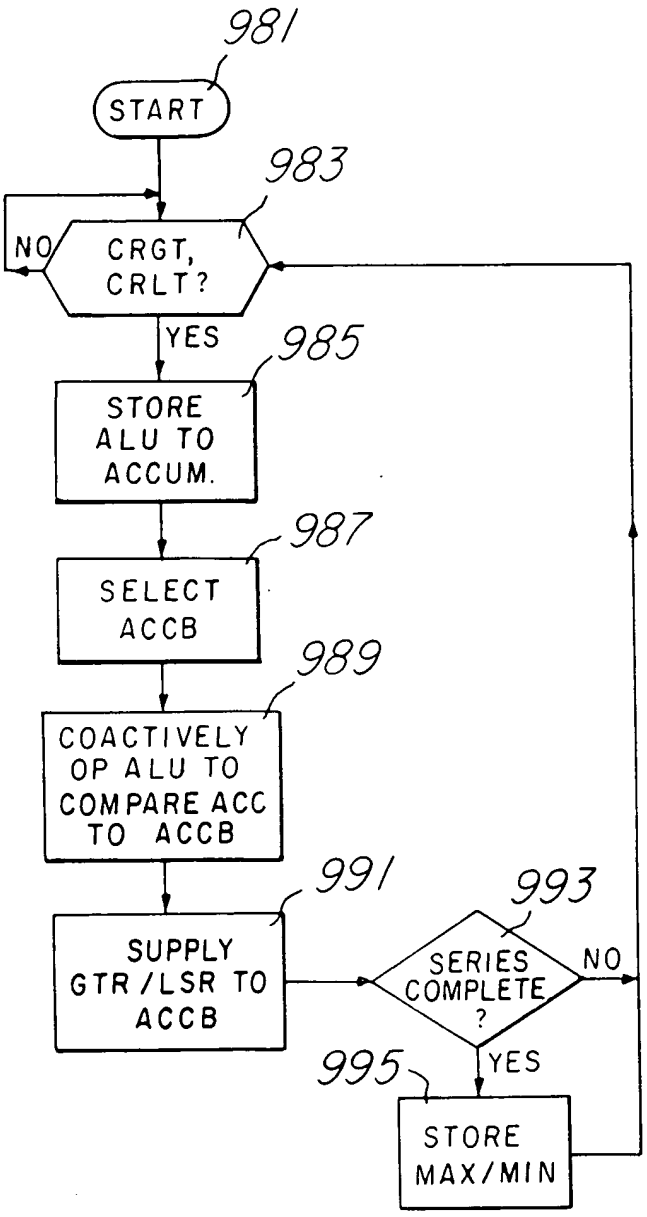

Fig. 28

00T60"8229960

PIPELINE

INSTRUCTIONS	CYCLE 1	2	3	4	5	6	7
1	FETCH	DECODE	READ	EXECUTE			
2		FETCH	DECODE	READ	EXECUTE		
3			FETCH	DECODE	READ	EXECUTE	
4				FETCH	DECODE	READ	EXECUTE
5					FETCH	DECODE	READ

Fig. 29

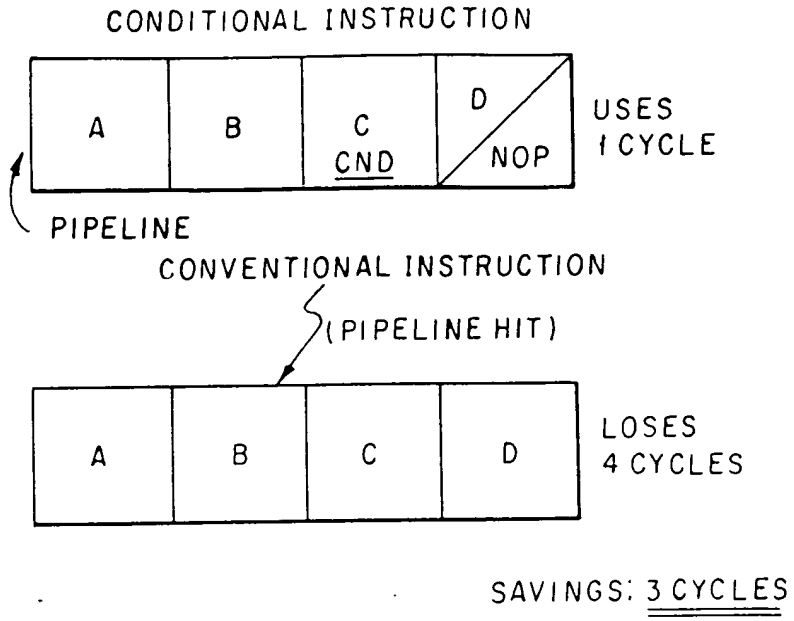
CONDITIONAL INSTRUCTION
A
B
C
CND
D
NOP
USES
1 CYCLE
PIPELINE
CONVENTIONAL INSTRUCTION
(PIPELINE HIT)
A
B
C
D
LOSES
4 CYCLES
SAVINGS: 3 CYCLES

Fig. 30

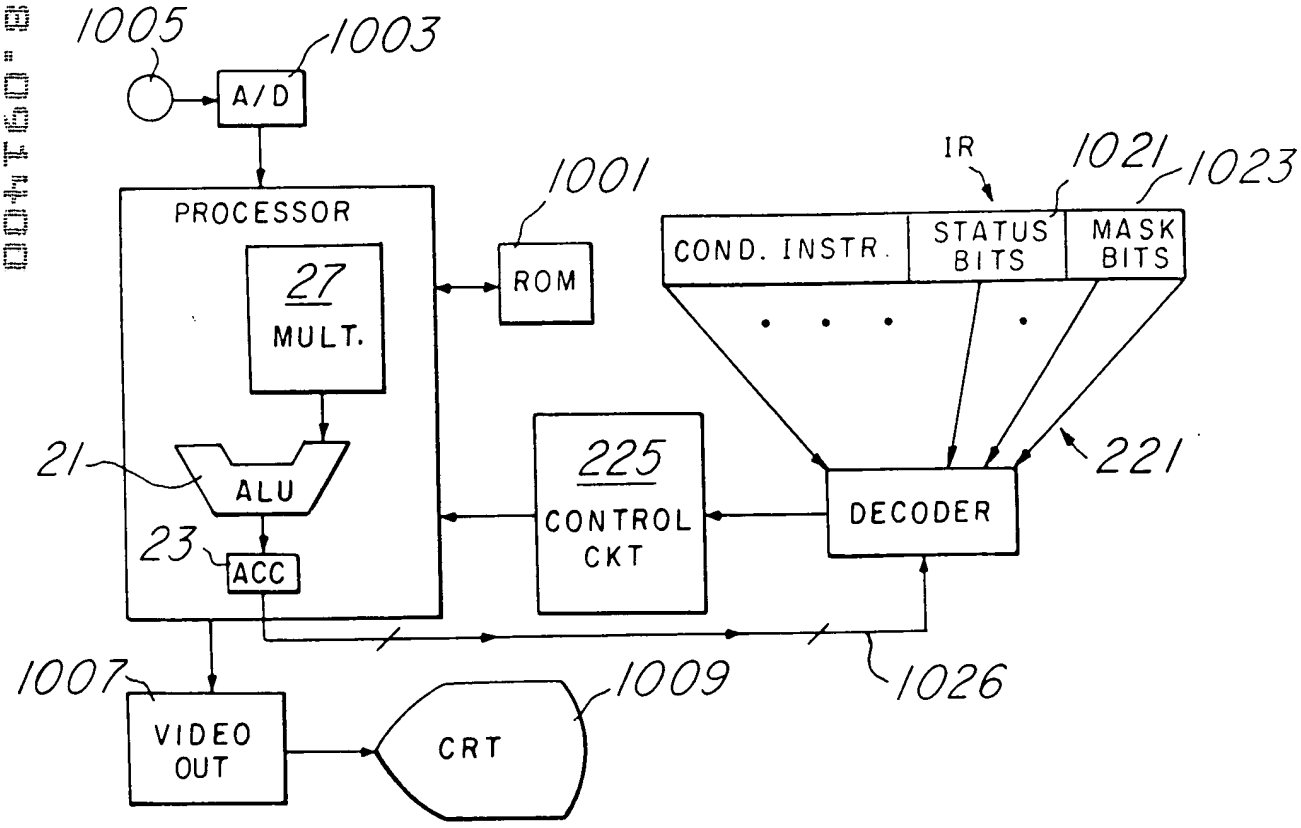
1005
1003
A/D
PROCESSOR
27
MULT.
1001
ROM
IR
1021
1023
COND. INSTR.
STATUS BITS
MASK BITS
21
ALU
23
ACC
225
CONTROL CKT
DECODER
221
1007
VIDEO OUT
CRT
1009
1026

Fig. 31

0050200 : 0050200

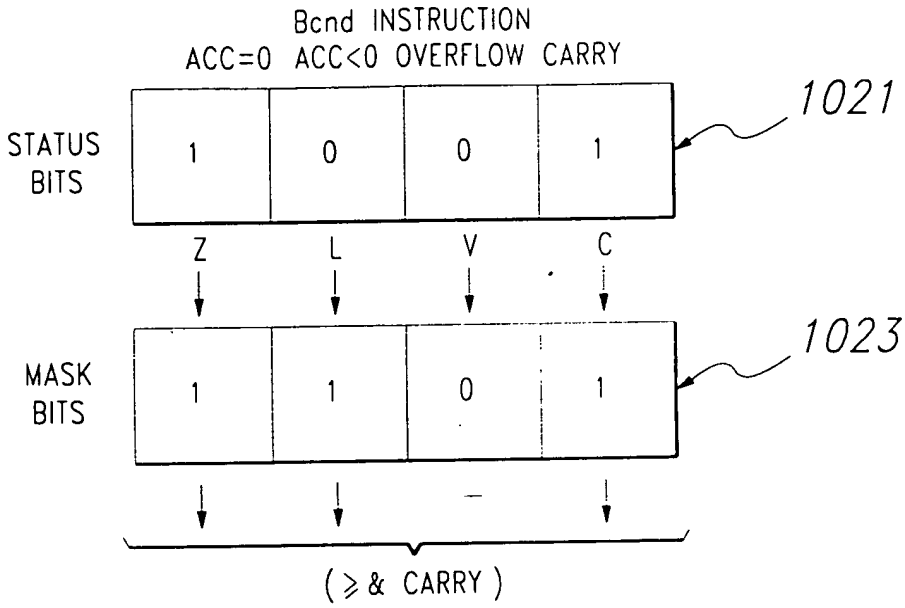

Fig. 32

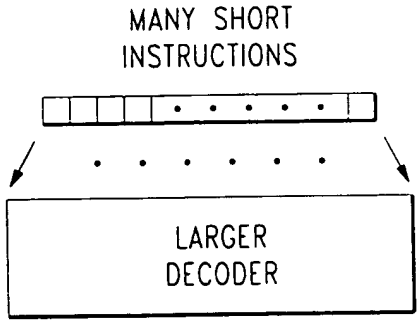

Fig. 33

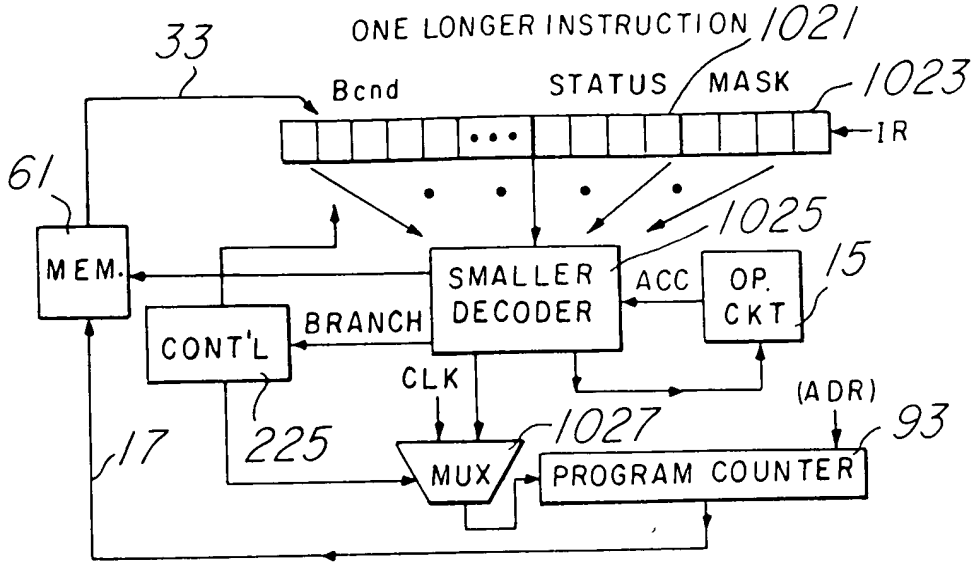
33
ONE LONGER INSTRUCTION
1021
Bcnd
STATUS
MASK
1023
IR
61
1025
MEM.
SMALLER DECODER
ACC
OP. CKT
15
CONT'L
BRANCH
CLK
(ADR)
93
17
225
1027
MUX
PROGRAM COUNTER

Fig. 34

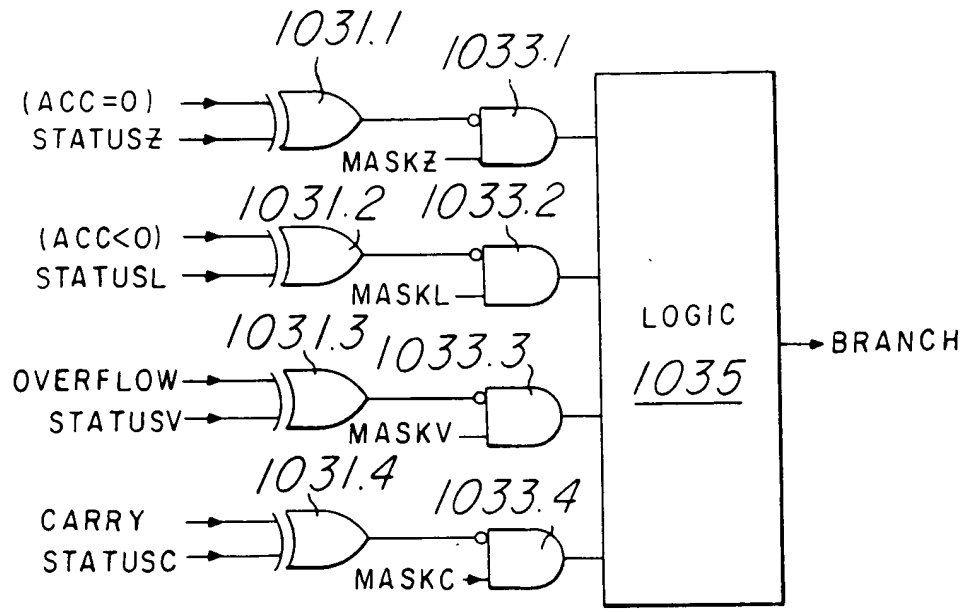
1031.1
1033.1
(ACC=0)
STATUSZ
MASKZ
1031.2
1033.2
(ACC<0)
STATUSL
MASKL
LOGIC
1035
BRANCH
1031.3
1033.3
OVERFLOW
STATUSV
MASKV
1031.4
1033.4
CARRY
STATUSC
MASKC

Fig. 35

0966228 0021400

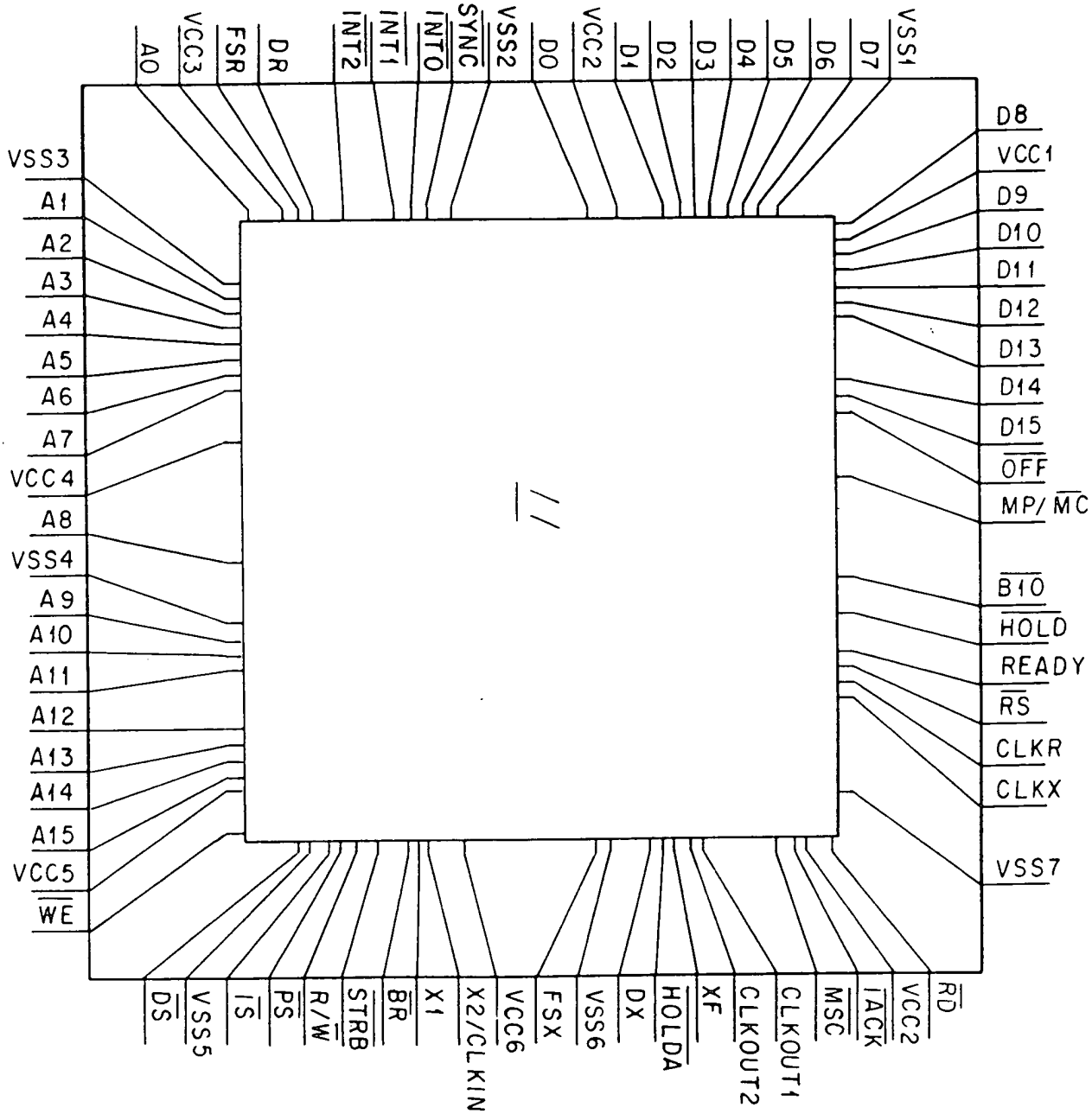

Fig. 36

00t760" 8222960

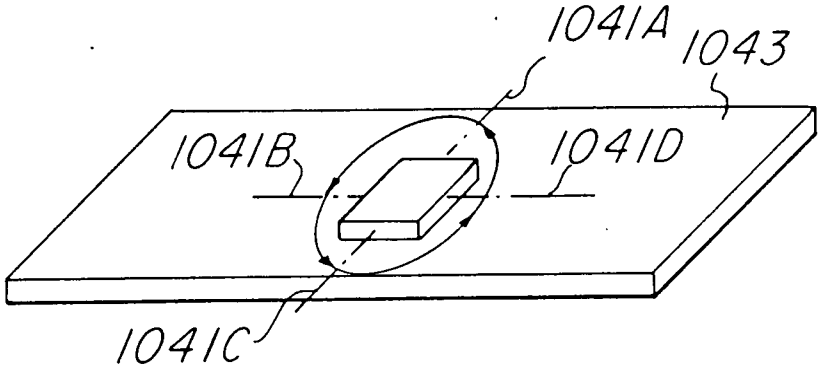

Fig.37

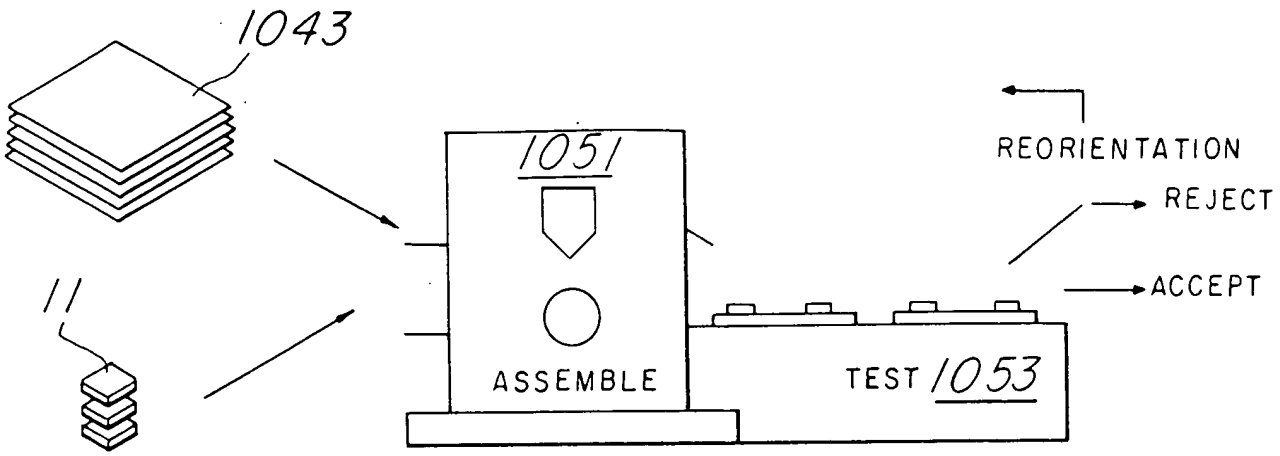
1043
1051
REORIENTATION
REJECT
ACCEPT
11
ASSEMBLE
TEST 1053

Fig. 38

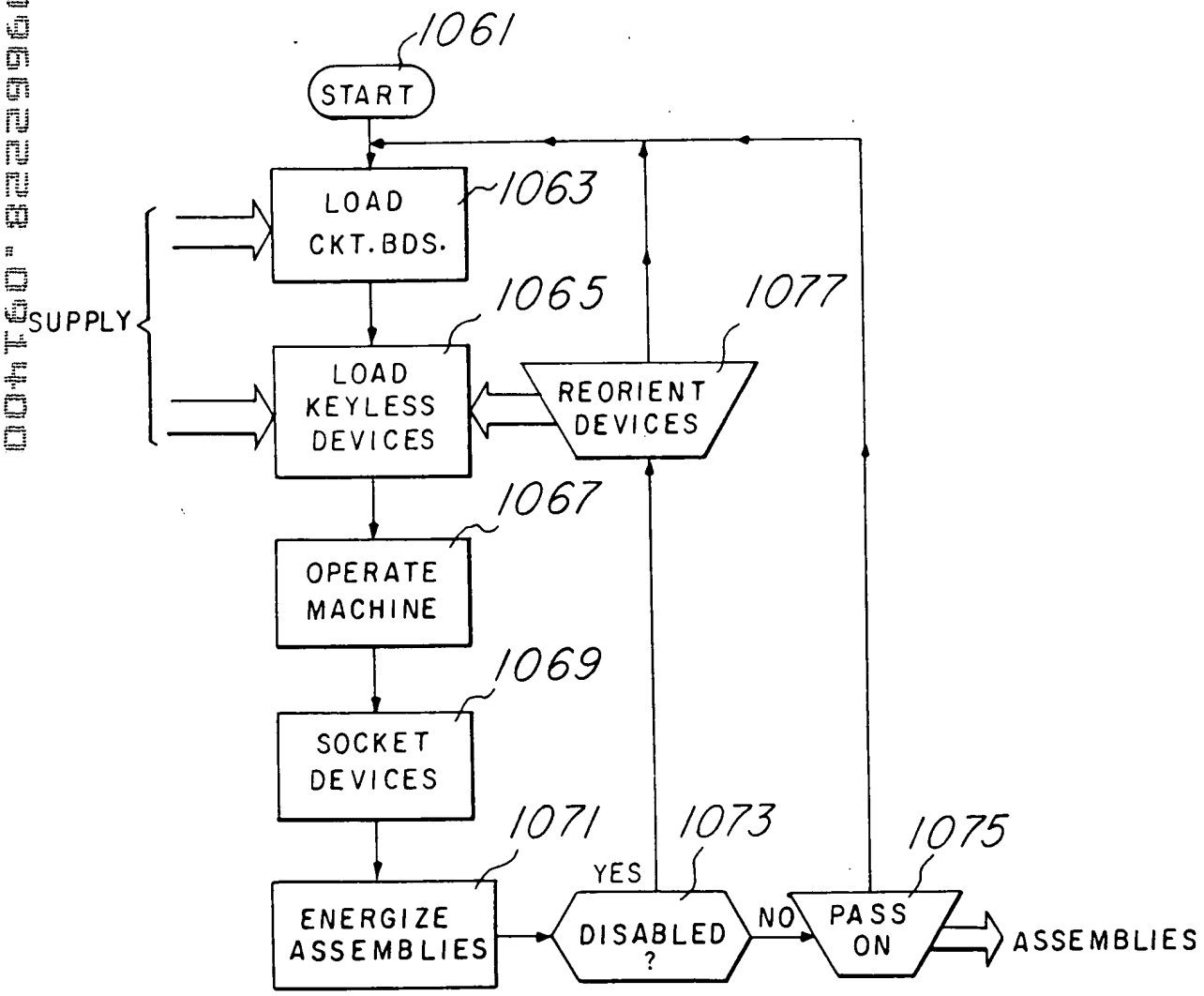
1061
START
LOAD CKT. BDS.
1063
SUPPLY
1065
LOAD KEYLESS DEVICES
1077
REORIENT DEVICES
1067
OPERATE MACHINE
1069
SOCKET DEVICES
1071
ENERGIZE ASSEMBLIES
1073
YES
DISABLED ?
NO
1075
PASS ON
ASSEMBLIES

Fig. 39

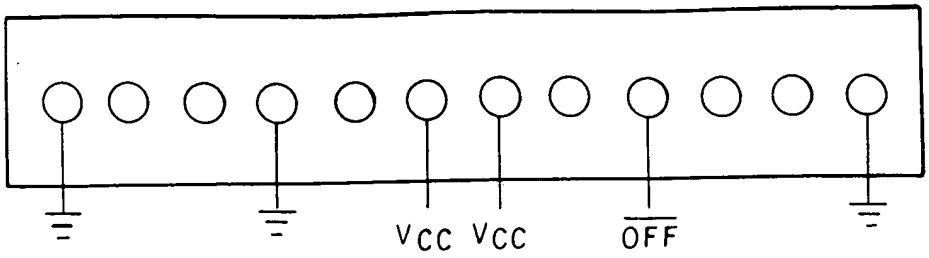

Fig. 40

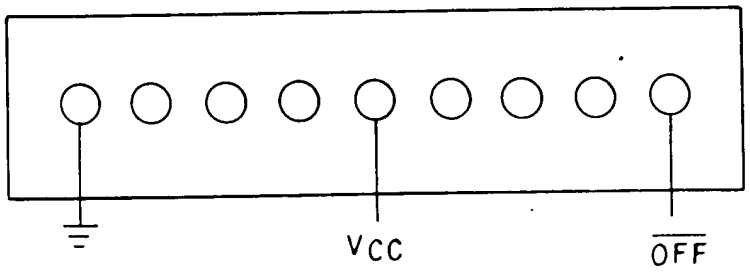

Fig. 41

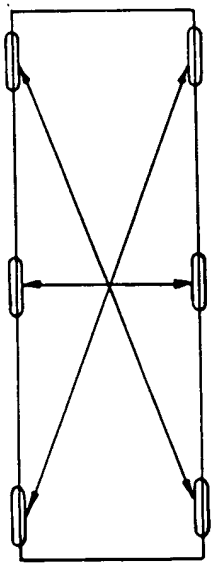

Fig. 42

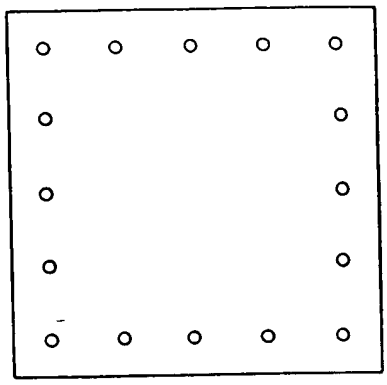

Fig. 43

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